Methods of Using Commercial Electromagnetic Simulators for Microwave and Millimeter-Wave Circuit Design and Optimization

Nitin Jain, *Member, IEEE* and Peter Onno, *Member, IEEE*

(Invited Paper)

***Abstract*— Efficient utilization of commercial electromagnetic (EM) simulators for design and optimization of microwave (MW) and millimeter-wave (MMW) circuits is achieved by classifying design problems into three categories—characterization of circuit elements, optimization of circuit elements, and creation of circuit element libraries such as scalable libraries. Practical aspects of the methods are illustrated by several examples. An equivalent circuit extraction technique suitable for n-port coupled structures is provided. The derived equivalent circuit is useful for extrapolating data, optimization, and deriving scalable models.**

***Index Terms*— Circuit optimization, electromagnetic analysis, microwave circuits, passive circuits.**

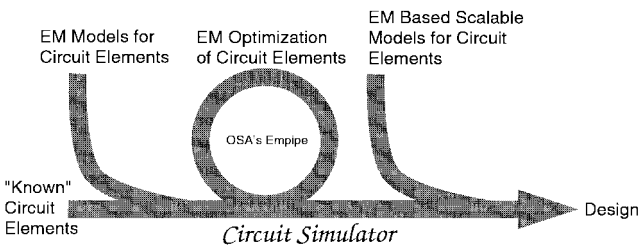


Fig. 1. Techniques commonly employed to utilize EM simulators for MW and MMW circuit design.

I. Introduction

In THE LAST few years, there has been a significant improvement in both computer resources (in terms of central processing unit (CPU) speed and reduced random-access memory (RAM) prices) and electromagnetic (EM) simulation software [1] so that use of commercial EM simulators has now become economically viable. As a result, there are now many commercially available EM simulation software packages. From the user's point of view, these packages are of two types. The first type is the two-and-one-half dimensional (2.5-D) solver using planar surface meshing but including vertical currents between layers, useful for planar structures such as microstrips (vendors include SONNET, Zeland, Hewlett-Packard, Ansoft, and Compact Software). The second type is the full three-dimensional (3-D) solver using volume meshing, appropriate for truly 3-D problems (vendors include Hewlett-Packard, Ansoft, and MacNeal–Schwendler). The 2.5-D software is based on the method of moments while the 3-D software is based on finite-element analysis or finite-difference in the spectral domain. Only recently has finite-difference time-domain (FDTD) software become available [2]. At M/A-COM, the authors have extensively used Sonnet's **em** [3], Ansoft's Maxwell SI Eminence [20], and HP's HFSS [4] to design and optimize microwave (MW) circuits. In this paper, the efficient use of these commercial EM simulators for MW and millimeter-wave (MMW) circuit analysis and synthesis will be considered. It will be assumed that the reader is familiar with the details of the software usage and their features (such as line/plane of symmetry) and concentration will be on problem formulation and solution. Some of the material included in this paper has been presented in past workshops [12], [21].

Broadly speaking, there are three methods of using the commercially available EM simulators for MW and MMW circuit design. These are predictive characterization of circuit elements for use in larger circuits, optimization of circuit elements for circuit performance requirements, and creation of dimensionally scalable library elements for use in integrated circuit design and modeling. Fig. 1 illustrates the three methods together with the relationship of the various EM simulation tools to the circuit simulators. While all three methods generate data that is used in a circuit simulator, EM-based optimization may also do more EM simulations depending on the results of the circuit simulators.

Of the three categories, predictive characterization of circuit elements is usually the most accurate, easiest to accomplish, and requires the smallest amount of computer resources. This is achieved by careful isolation of the unknown structure from the known structures to reduce the problem size. For any EM simulation, it is very important to look ahead in terms of software requirements. The problem may have to be slightly modified, usually dimensionally, so that it is optimized for the software to be used; this can further reduce computation time. This issue will be discussed in some detail in Section II where

Manuscript received June 3, 1996; revised November 12, 1997.

The authors are with M/A-COM, Inc., Corporate R&D Center, Lowell, MA 01853 USA.

Publisher Item Identifier S 0018-9480(97)03103-7.

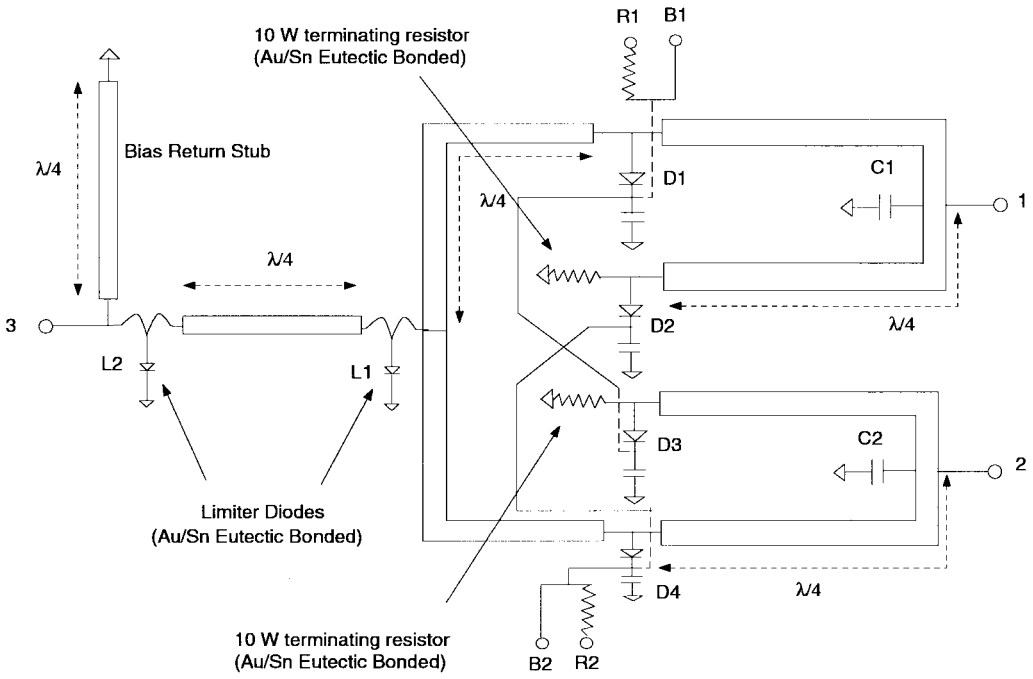


Fig. 2. Schematic of an integrated switch limiter.

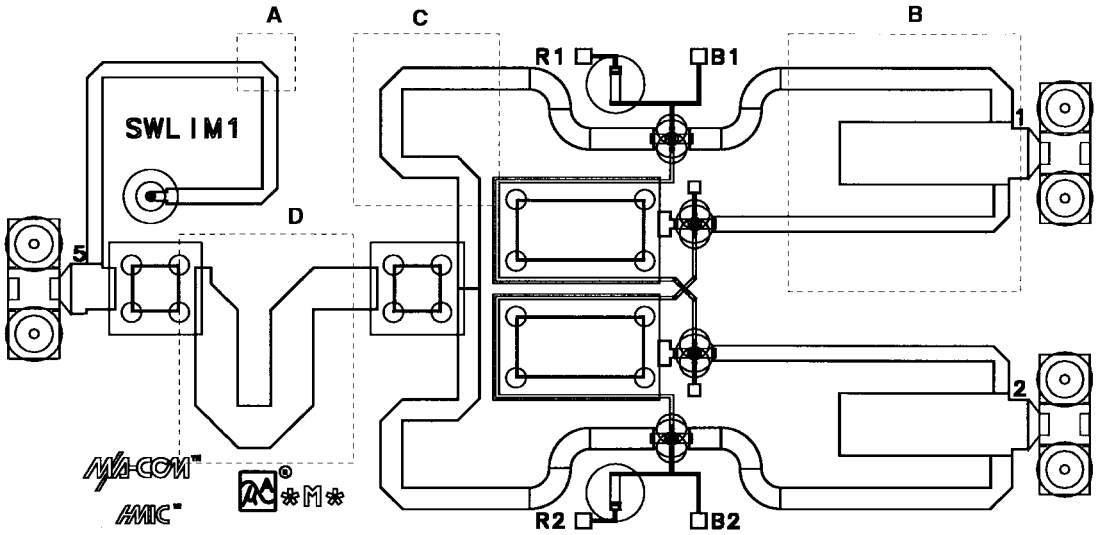


Fig. 3. Switch-limiter layout in HMIC. The dotted regions represent geometries that were simulated in the Sonnet's **em**. The S-parameter data as simulated and de-embedded in Sonnet's **em** was imported into MDS and the other known elements optimized to give the optimum overall circuit performance.

two examples of predictive characterization of discontinuities are demonstrated.

If the computed EM characteristics of the circuit element do not satisfy the overall circuit performance requirements, the geometry of the element needs to be modified. In such situations, numerous EM simulations are conducted to optimize the circuit element. In Section III, optimization of circuit elements using commercially available software is considered.

Circuit element optimization can be performed by either structural optimization or by dimensional optimization. Structural optimization refers to fundamental change in geometry, such as addition of new metal and dielectric patterns, while dimensional optimization refers to the modification of physical dimensions, such as length of a given metal and dielectric patterns. In Section III, structural optimization is first considered by utilizing various parameters such as field distribution, cross-coupling capacitors, and S-parameters and new structures for optimum performance are developed. Next, dimensional optimization is considered, where dimensions of a given structure are optimized. While parametrized and scalable equivalent circuits have been extensively used for dimensional optimization, recently, direct optimization using EM simulations has been demonstrated with improved optimization

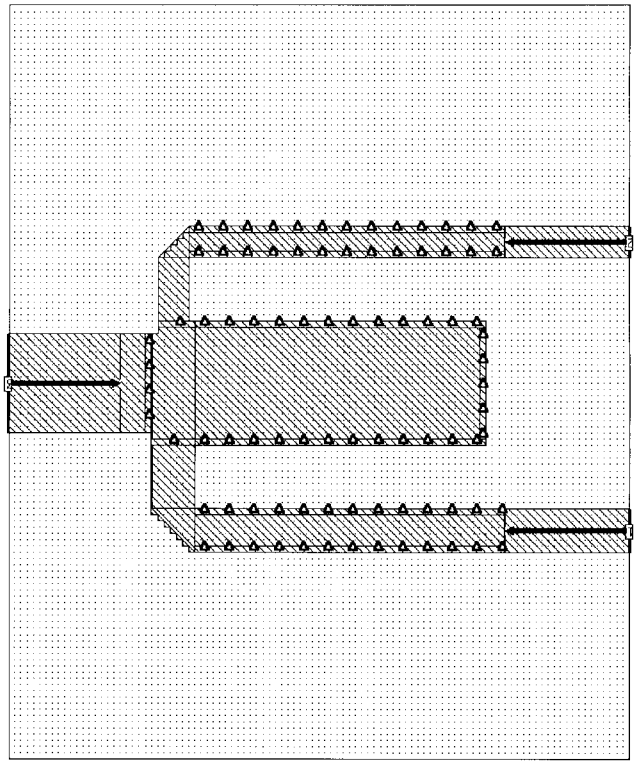


Fig. 4. The Sonnet layout for the three-port open-stub capacitance utilized to provide low loss.

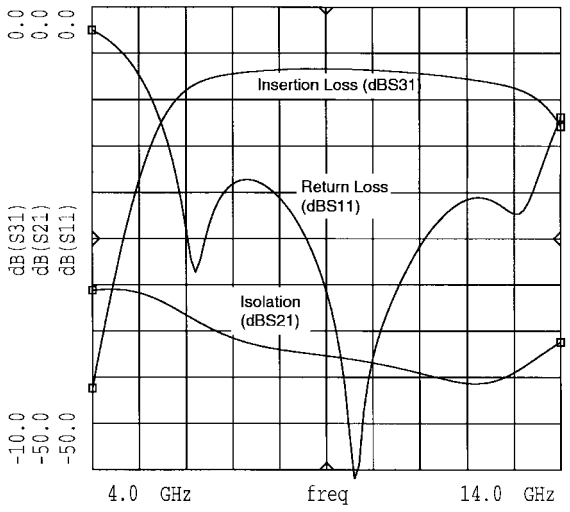


Fig. 5. Simulated response with S-parameter from Sonnet's EM used in conjunction with MDS models.

algorithms [5], [6]. A commercial software package, OSA's Empipe [7], has UNIX-based links to Sonnet's **em** to optimize a given structure using EM simulations. These new methods are efficient and examples of automatic circuit optimization using OSA's Empipe will be given.

Even though the methods outlined above are capable of solving many MW problems, there are situations where circuit element building blocks are required for MW circuit design. Often these are accommodated in library wafer runs which are

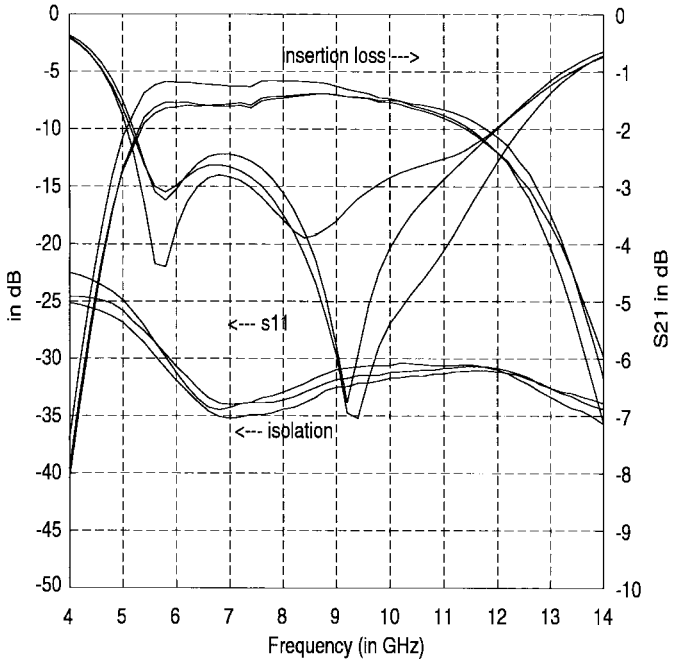


Fig. 6. Measured S-parameter for a switch-limiter. First iteration with no tweaking.

processed, measured, and modeled. However, as circuits are stressed to their performance limits, there is a continual need for process changes and novel circuit-element designs that improve circuit performance with improved yields. In a typical commercial environment, timely need for new library elements is most critical and often there is insufficient time for wafer runs to characterize new ideas. In such situations, a number of batch EM simulations are conducted—sometimes over a week or two—and dimensionally scalable library models are extracted. In Section IV, two examples of scalable circuit libraries are presented.

II. Characterization of Circuit Elements

In this section, a glass-based integrated circuit is first considered which shows how various elements in the circuit are characterized using EM simulations. The second example considers a surge protector for commercial frequencies illustrating predictive design to provide the required bandpass response. For reference, the glass microwave integrated circuit (GMIC) cross section is shown in Appendix I [8], [9].

Example 1—HMIC Switch Limiter: Fig. 2 shows the schematic for a matched 7–11 GHz single-pole double-throw (SPDT) switch in series with two stages of limiters. The bias of the diode labeled D_1 is tied to D_3 while that of D_2 is tied to D_4. Thus, when D_1 and D_3 are reverse biased and D_2 and D_4 forward biased, the signal from terminal 1 goes to terminal 3 while the signal from 2 is terminated in a high-power AlN resistor. The through path as well as the terminating path are simultaneously implemented as asymmetric commensurate line filters modified by capacitive loading [10], [11]. For the through path there is a shunt stub followed by two series quarter-wave sections and then a shunt

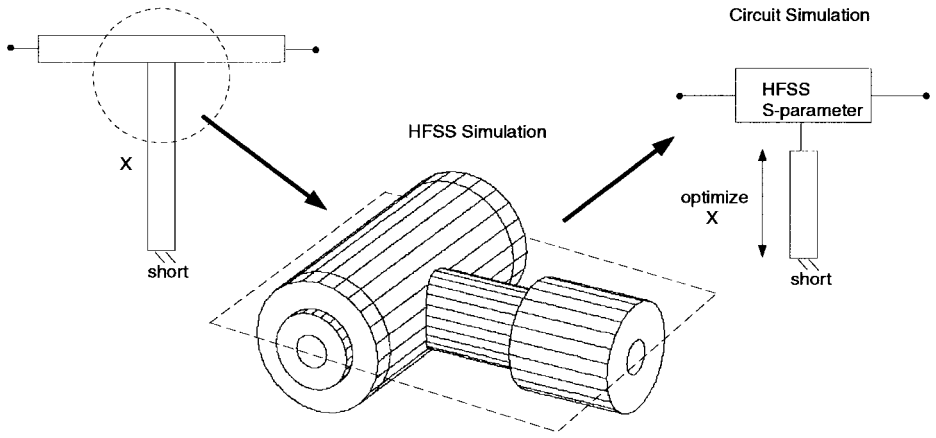


Fig. 7. A coaxial surge protector designed with the help of HFSS simulations.

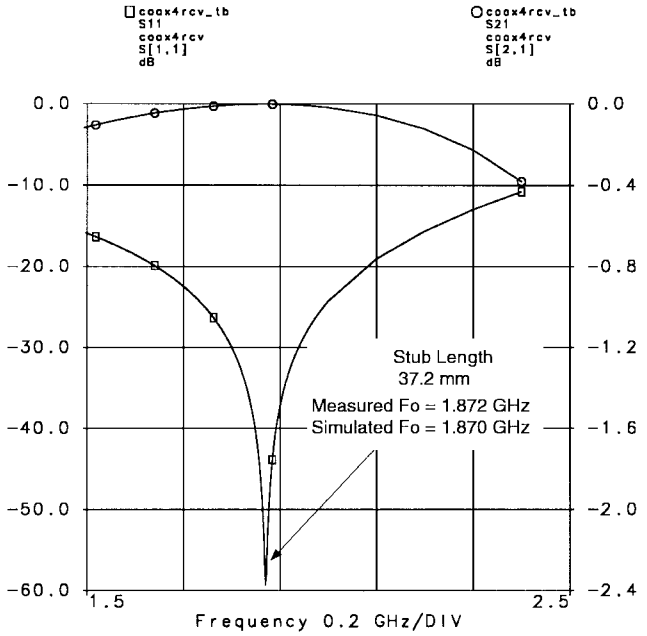


Fig. 8. Simulated response of a coaxial filter. The measured F_o is within 2 MHz of the filter response resonance at 1870 MHz.

Resonant Frequency (GHz)	
Measured	Simulated
1.541	1.516
1.807	1.790
1.872	1.870
1.902	1.900
1.917	1.911
2.035	2.047
2.107	2.136

Fig. 9. Table illustrates other designs and compares measured with simulated F_o.

stub followed by another series section and a bias return shunt stub. Thus, the through path represents an order 4 filter while the terminating path is an order 2 filter; this is dictated by the circuit topology.

This circuit was implemented in heterolithic microwave integrated circuit (HMIC) technology [8], [15]. The p-i-n diodes marked D_1-D_4 are integrated in HMIC while the limiter p-i-n diodes marked L_1 and L_2 are chips bonded on the HMIC. The limiter diodes were not implemented in HMIC as the optimum I-region thickness required by the two limiter diodes are different from each other and from that of the integrated switch diodes D_1–D_4. The diodes have nonzero capacitance, which is incorporated in the filter using standard techniques [10], [11].

Fig. 3 shows the layout of the matched switch limiter as implemented in HMIC. The capacitors at terminals 1 and 2 were implemented by open-circuit stubs. The limiter diodes and the terminating AlN resistors are mounted on pedestals. The switch diodes are implemented in HMIC and have a well-controlled capacitance of 0.08 pF.

When the circuit was laid out in the allocated space, it was soon discovered that there were many circuit elements which were unknown and required characterization as they were critical for the circuit performance. In particular, the size forced the authors to bend lines outlined by the dashed boxes in Fig. 3 labeled *A*, *D*, and *C*, while loss forced us to use wide stubs as in box *B* instead of the inherently more lossy metal–insulator–metal (MIM) capacitors. Characteristics of these structures were inadequately represented in the linear circuit simulator and required EM simulations.

After the initial design using Hewlett-Packard's circuit simulator MDS, a layout similar to, but dimensionally different from that in Fig. 3, was obtained by using the auto-layout functionality in MDS. Since Sonnet requires geometries to be defined on grid points, the authors' initial designs were all adjusted for inclusion in Sonnet. Thus, the greatest common

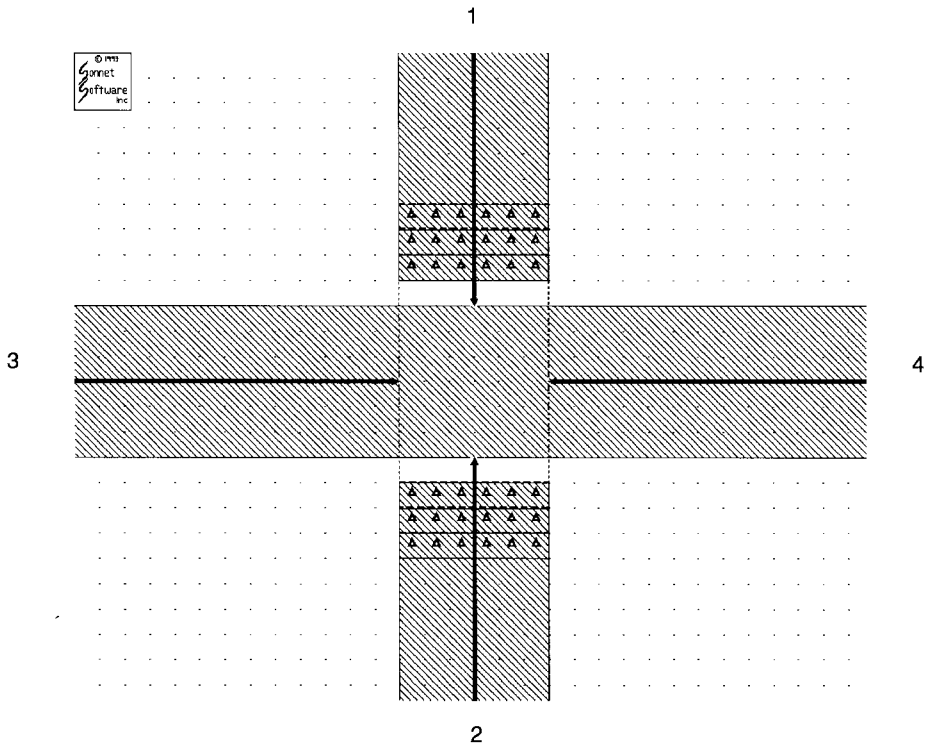


Fig. 10. A simple crossover. The lines need to be 3-mil wide to allow for high-power handling.

factor for each dimension in substructures *A–D* was made to be as high as possible. For example, for the element outlined in box *B* the factor of choice was 1 mil, which means all dimensions were integer multiples of 1 mil. The large grid size reduces the number of subsections, thus speeding up EM calculations. The grid requirements for fast EM simulations imposed minimal restriction on the design itself or on the design method.

The structures *A–D* were then simulated in Sonnet and the data was imported into the circuit simulator (MDS). For example, Fig. 4 shows the Xgeom (Sonnet's layout package) drawing of the circuit element represented in structure *B* of Fig. 3. Since metal in Sonnet is represented by zero thickness of nonzero sheet resistance, the effect of metal thickness is simulated by including two layers of thin metals separated by air dielectric equal to the metal thickness and connecting the two metal layers together by edge vias, represented in Fig. 4 by the downward pointing triangles. This technique produces a rectangular cavity with the correct metal boundary for inclusion in Sonnet. The extra length of line on either side of the geometry is utilized to keep the distance of the structure of interest two to three substrate thicknesses away from the box wall in Sonnet. This avoids interference of the simulation box with the structure. The structure in Fig. 4 took 39 Mbytes of memory requiring 2200 subsections and took 11 h for 21 frequency points on an HP 735 workstation. Simulation times on the other structures were shorter, and all of the structures used in this circuit could be simulated over a single weekend.

The S-parameters obtained from Sonnet simulations were combined with the other element models available in MDS

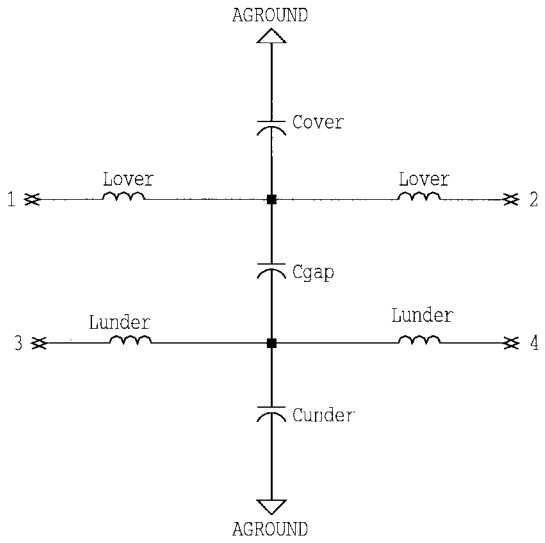


Fig. 11. The equivalent circuit of the de-embedded crossover. The elements of the circuit were obtained from even- and odd-mode analyses as shown in Fig. 12.

to optimize the circuit to obtain the performance shown in Fig. 5. The length of the stub is fixed, thus fixing the loading capacitance; however, the dimensions of the series lines and the diode capacitances provide enough free parameters to obtain the required performance. Fig. 6 shows the measured performance of the switch limiter. The simulated performance differs from the measurements because the attached limiter diodes had 0.15-pF capacitance instead of the 0.10 pF required for the filter structure. The measured isolation is lower in Fig.

6 (>30 dB instead of 40 dB) because the line coupling between terminals 1 and 2 was not modeled. However, the isolation met the specifications and was not a serious issue. Since the HMIC diodes are well modeled the deviation in the loss calculations was less than 0.2 dB in the 7–11-GHz bandwidth. These results represent first iteration measurements with no tweaking and demonstrate the success and the value of EM simulators.

Example 2—Coaxial Surge Protector: Surge or lightning protectors are often used in front of sensitive equipment. They typically have narrow passband response and are usually implemented with a shorted stub to ground. This example shows how a coaxial surge protector can be designed for any frequency by doing a single EM simulation.

Fig. 7 shows the principle behind the EM-based design of the coaxial surge protector. The circuit functionality is very simple; the coaxial short presents an open circuit to the signal line at the operating frequency. The prediction of the resonant frequency is very difficult because the coaxial T-junction is quite complicated and its frequency behavior unavailable. To solve the problem efficiently, the coaxial surge protector is divided into two parts—the unknown T-junction and the known lines connected to it.

The T-junction is drawn in HFSS. The ports are defined sufficiently far from the junction so that evanescent modes have minimal effect on the characterization. Symmetry can be used to reduce simulation time; however, in this case, the drawing was asymmetric and, therefore, a full structure simulation was required.

Since the frequency range of interest was 900–2500 MHz the authors adaptively meshed the structure at 2500 MHz in HFSS. The structure went through six adaptive passes with 20.5 K tetrahedra occupying 264 Mbytes of RAM and taking 5 h 40 min of CPU time on an HP 735 UNIX workstation. The overall computer time is usually more than the CPU time as there are significant read/write processes during the overall adaptive calculation. Each subsequent frequency calculation took 1 h 35 min. The accuracy of the simulation was very important and, therefore, the T-junction was finely meshed.

Since HFSS usually takes much longer with loss calculations at these frequencies, the simulations assumed ideal lossless materials. The frequency sweep function is used to simulate the T-junction response for 100 MHz steps in 900–2500-MHz band. Since the T-junction S-parameters were very well behaved (since the discontinuity is well approximated as lumped element) the authors did not have to simulate any finer frequency steps; the linear circuit simulator (HP-EEsof) interpolated the data accurately.

Fig. 8 shows the simulated bandpass response of a typical coaxial surge protector. This simulation is obtained through a linear simulation (in HP-EEsof's Libra IV) by combining the HFSS simulated S-parameters of the T-junction with that of the standard coaxial transmission line model available in HP-EEsof's linear circuit simulator. For comparison, the simulated and measured resonant frequency for seven such surge protectors are tabulated in Fig. 9. The measured resonant frequency is within 2% of the predicted values between 1.5–2.1 GHz. Once the T-junction is characterized, the optimization of the surge protector for any frequency is very efficient and completed

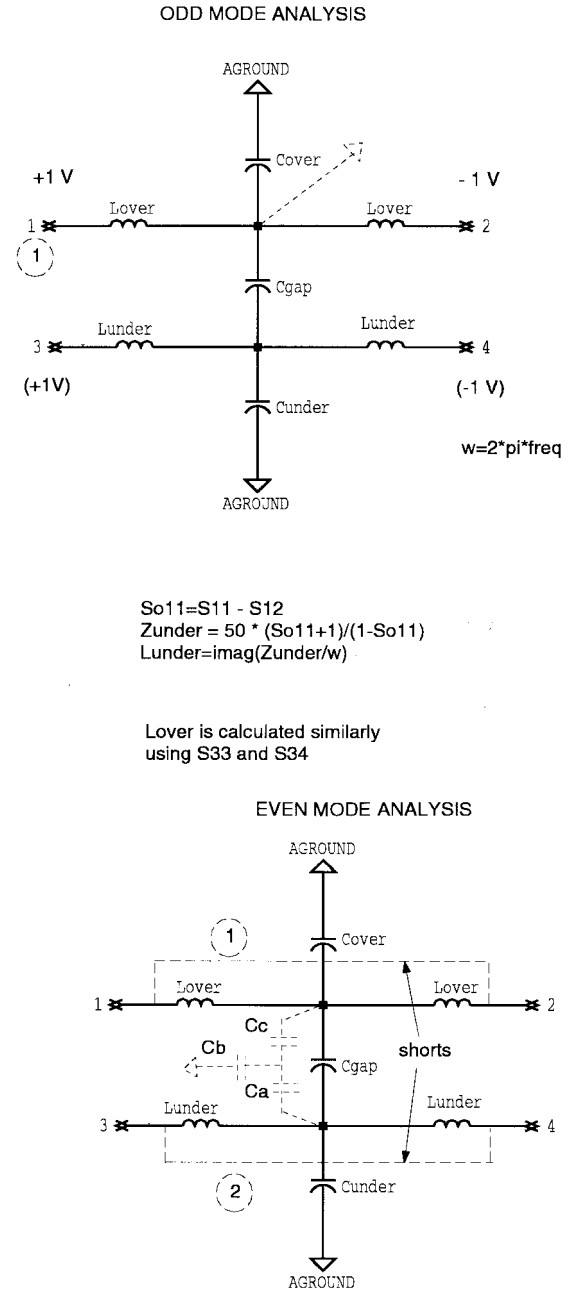


Fig. 12. The extraction of the equivalent circuit of the crossover. Odd- and even-mode calculations are conducted for each frequency point and the equivalent circuit is obtained in closed form in MDS's presentation page.

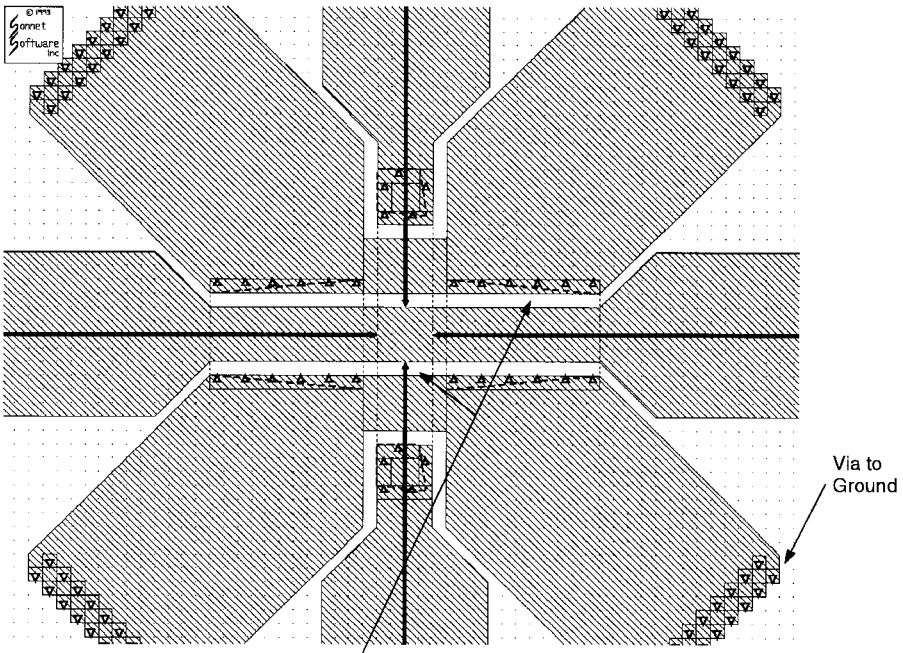


Fig. 13. The optimized crossover. The Xgeom layout shows only one layer. The dotted lines indicate the metallization above this layer while the up pointing arrow represent the airbridge posts.

entirely in the linear circuit simulator. Also, note that the simulated data for the coaxial T-junction is generic and usable for other designs.

III. Optimization of Circuit Elements

In the previous examples, the circuit elements provided the required response for optimization of the overall circuit. There are many situations where the unknown circuit elements can degrade the performance of the overall circuit and optimization of only the known circuit elements is inadequate. In such situations, optimization of the circuit element to meet the requirements of the overall circuit is required. This section considers five examples that illustrate the use of EM simulators for circuit element optimization.

Examples 3 and 4 in this section illustrate optimization of circuit element structures. Example 3 is a high-power high-isolation RF crossover where the S-parameters are analyzed to help add critical metal patterns to increase isolation. Example 4 shows the optimization of a surface mount connector by utilizing EM field plots.

Examples 5–7 illustrate optimization of the dimensions of circuit elements. Example 5 is an interdigital filter where 2-D EM simulation of the cross section is used to optimize a linear phase filter. This example illustrates the importance of 2-D simulations for accurate calculation of coupling and impedance. Example 6 illustrates coplanar structures where automation in the optimization is achieved via the use of Empipe. Finally, Example 7 illustrates the design of a 3-dB backward coupler which required extraction of the equivalent circuit to determine the suitability of a given structure for automated optimization. The structure was slightly modified and automatic optimization was accomplished with Empipe.

Example 3—Crossover in HMIC: High-isolation (>40 dB) and high-power (∼10-W CW) microstrip RF crossovers at greater than 10 GHz are difficult to fabricate. In this example, a design method is illustrated to obtain such a crossover in GMIC (see Appendix I). The crossover has been utilized in the design of a high-power switch with about 40 dB of isolation over 6–18 GHz [10], [14].

Fig. 10 shows a layout of a 3 × 3 mil crossover drawn in Sonnet's Xgeom which was simulated and de-embedded by Sonnet's **em**. The S-parameters generated by Sonnet were analyzed to derive the four-port lumped equivalent circuit shown in Fig. 11. There are no mutual inductances between the orthogonal lines. The key parameter in the equivalent circuit is the capacitance, $C_{\rm gap}$, as that determines the isolation. The various elements of the equivalent circuits are obtained by performing even- and odd-mode analysis, converting the even- and odd-mode S-parameters to Z-parameters and, thereby, determining the reactance and susceptance of the elements. This extraction process of the equivalent circuit is shown in Fig. 12. Since the coupling between the lines is determined by the capacitance, $C_{\rm gap}$, for increased isolation it is important to minimize $C_{\rm gap}$.

Though the crossover in Fig. 10 could handle 10-W CW power, Sonnet simulations indicated that the coupling capacitance with 5-μm airbridge is 24.3 fF (parallel plate capacitance is 10.3 fF while the fringing near the crossover is estimated to be about 4.2 fF and the capacitance between the approaching

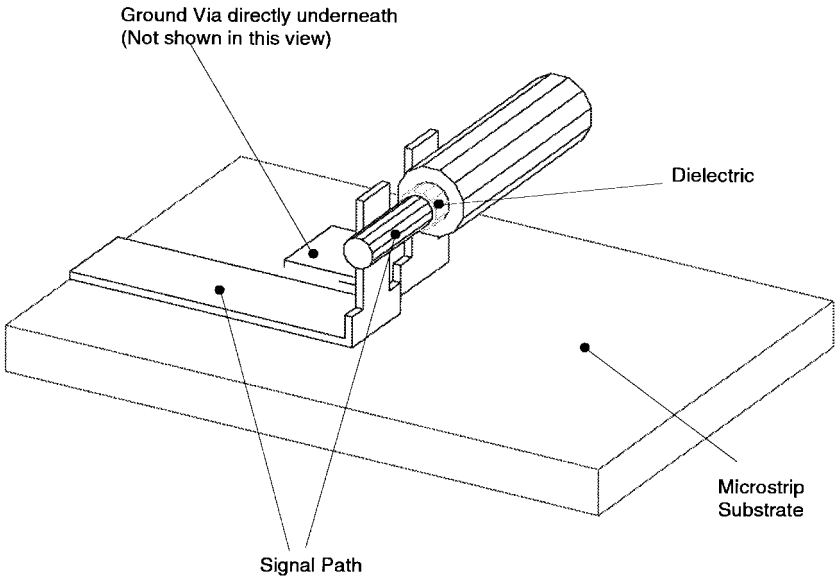


Fig. 14. A plastic surface mount connector. Outer plastic housing is removed to show the inner layout. Ground via is hidden in this perspective.

lines not due to the crossover is 9.7 fF). This value of the coupling capacitance is too large to provide the required isolation.

Inserting shield metallization which is RF grounded between the lines, 0.5 mil away from the lines, decreased the coupling capacitance by about 6.5 fF by reducing the line-to-line capacitance. Reducing the 0.5-mil separation to 0.25 mil decreased $C_{\rm gap}$ marginally; however, the smaller gap is more demanding of the fabrication process. Therefore, it was decided to keep the ground shields 0.5 mil away from the lines.

To further reduce the coupling capacitance, the width of the lines at the crossover was reduced from 3 to 1 mil. The power handling is somewhat compromised but since the 1-mil section is very short, thermal heating due to resistive losses remained low even at 10-W incident power. This was verified by thermal analysis and experimentation. By reducing the line widths to 1 mil at the crossover point the parallel plate capacitance is reduced to 1.1 fF from the initial value of 10.3 fF. The smaller linewidth also decreased the fringing capacitance at the crossover. Finally, grounding straps were introduced in order to pass ground in parallel at the underpass to further reduce the overall fringing capacitance of the crossover.

The Xgeom layout of the final crossover is shown in Fig. 13. During the process of optimization, some fifteen different crossovers were simulated; the dimensions were varied to find the optimum geometry. The optimized crossover has a predicted $C_{\rm gap}$ capacitance of 3.5 fF which compared very well with the measured value of 4.0 fF. The differences between the two values are due to: 1) omission of metal thickness in the simulation and 2) the variance in the crossover height from the nominal value of 5 μm.

In summary, this example showed a factor of almost seven reduction in the coupling capacitance. This translates to an increase of 17 dB in the isolation.

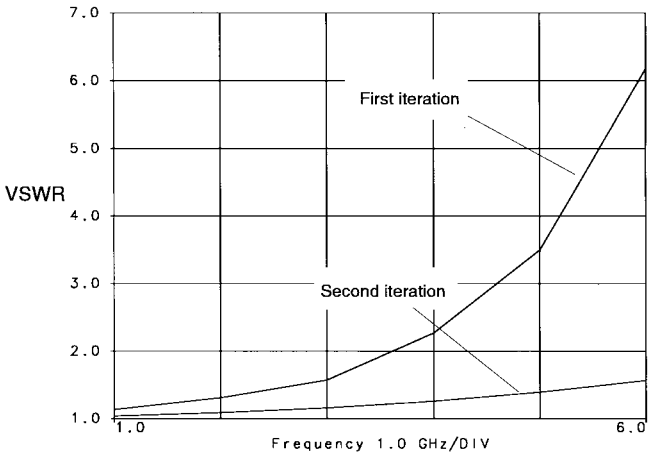


Fig. 15. HFSS simulations. The first simulation represents the nonoptimum connector, while the second is the optimized connector using field plots in Fig. 16.

Example 4—Surface-Mount Connector: High-volume MW and MMW commercial applications are demanding more compact, cheaper, and better performing connectors. This has greatly affected the method of manufacturing connectors. The first step of prototyping can now be done using 3-D EM simulation packages. Besides reducing cost and manufacturing time, EM simulations increase everyone's understanding of connectors.

Fig. 14 shows a conceptual surface mount connector that acts as a coaxial-to-microstrip transition. To reveal the details of the connector, the plastic surrounding the connector is not shown. The ground via in the microstrip substrate connects the coaxial ground to the microstrip ground. This via is some distance from the plastic housing and is not visible when looking down at the connector. The coaxial feed and the microstrip line are both designed to have an impedance of

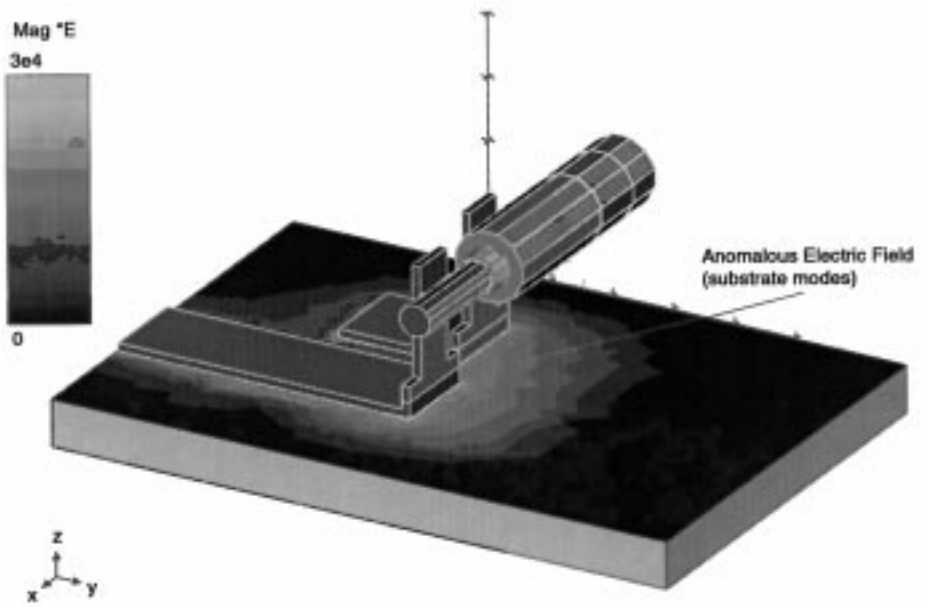


Fig. 16. Time average of the magnitude of electric field plotted on X–Y plane illustrating anomalous electric field close to ground electrode. This showed that the ground path of the connector was too long.

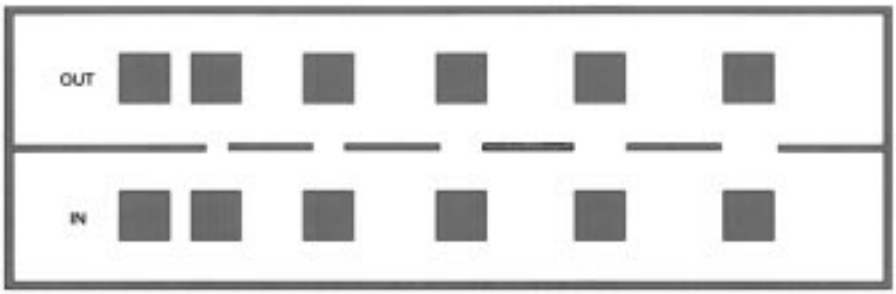


Fig. 17. Interdigital filter cross section. Nonadjacent coupling is provided by the four leftmost slits.

50 Ω, with the connector required to have low VSWR for frequencies as high as 5 GHz. The connector was drawn and simulated in HP's HFSS.

The initial design did not meet the performance requirements. Since connector specifications are usually given in VSWR, Fig. 15 shows the simulated VSWR going up to 6:1 at 6 GHz. Addition of known circuit elements such as open stubs to improve the match proved futile; therefore, the authors proceeded to examine the connector itself in more detail.

Fig. 16 shows the time-averaged magnitude of the electric fields in the X–Y plane at the interface between the microstrip and the coaxial connector at 6 GHz. Clearly the electric field patterns near the ground path on the substrate are anomalous and are believed to be due to substrate modes being excited by the long ground path. Moving the ground via closer to the line substantially reduced the spurious surface modes, improving the VSWR as shown by the trace marked "second iteration" in Fig. 15. Standard circuit matching techniques were used for final realization.

The optimization examples considered so far in this section required fundamental changes in the structure; for example, ground shields were introduced to increase the crossover isolation. Such changes are at the macro level where the structure itself is being modified. Very often, as in filters, there

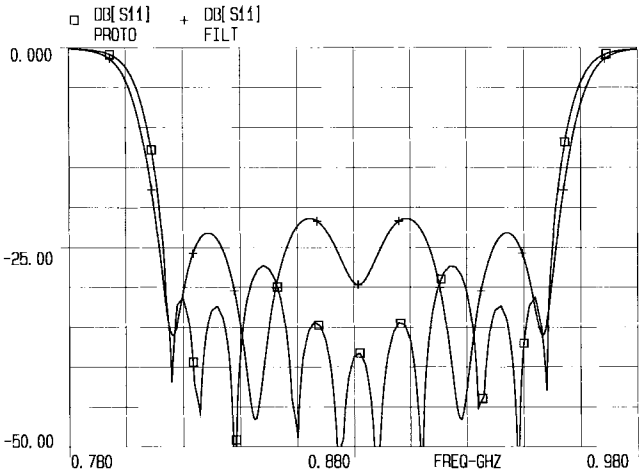


Fig. 18. Return loss for prototype and filter derived from initial 2-D simulation.

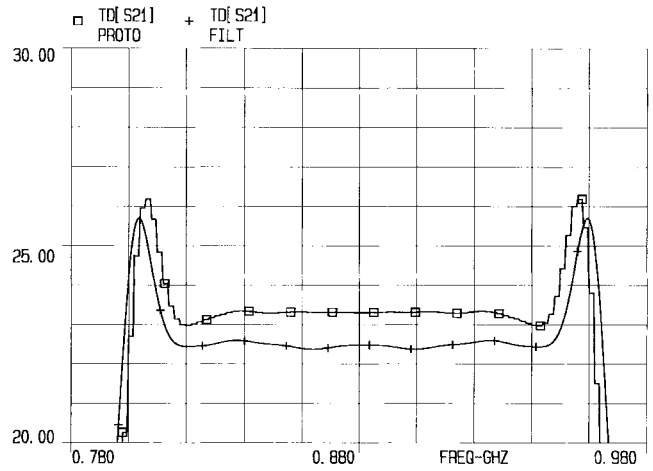


Fig. 19. Group delay for prototype and filter derived from initial 2-D simulation.

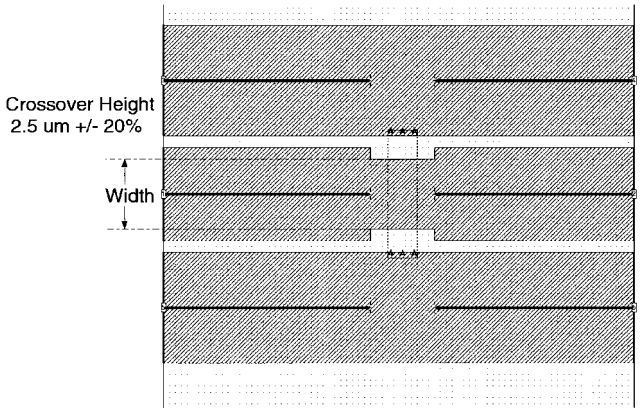


Fig. 20. Ground equalization straps in CPW.

are well-defined structures whose dimensions are modified to obtain an optimum performance. Dimensional optimization is as important as structural optimization; often structural optimization can be accomplished by a good understanding of the problem. There are a number of ways of accomplishing dimensional optimization; one known to the authors is due to OSA, Inc., through the use of their software called Empipe [7]. Empipe uses UNIX-based pipes to established a link between Sonnet's Em and a proprietary optimization algorithm. The algorithm conducts EM-based experiments through Empipe and uses the results to optimize the specific dimensions.

Example 5—Interdigital Filter: The design of coupled line filters has long benefited from the design curves presented in [18]. The cross section of a linear phase interdigital filter is shown in Fig. 17. Its design is complicated by the introduction of slit coupling between nonadjacent resonators along with the usual adjacent bar coupling. This example provides a procedure which utilizes 2-D EM simulations to manually optimize the filter to the required specifications.

The design process began with a quarter-wave stub-line implementation using the low-pass prototype element values presented in [19]. The match was optimized using a netlist circuit simulator. The initial equal-stub version was then transformed to an identical-bar implementation using an iterative loop of successive Kuroda transforms constrained by functions derived from Getsinger's curves. The resulting cross section was simulated with Maxwell 2-D [20] to obtain a better approximation for the capacitance matrix.

Return losses for the optimized prototype and a filter whose elements are derived from the Maxwell simulation are plotted in Fig. 18 and the corresponding group delays in Fig. 19. There are significant differences resulting from the effects of multiple bars as well as the approximations associated with the coupling slits. The desired coupling coefficients were obtained after a couple of manual iterations since each simulation provided sufficient information for the capacitance values as a function of bar gaps and slit widths to adjust the dimensions for the next iteration.

While 3-D EM simulation was useful for investigating end effects and other discontinuities, getting accurate results for the whole filter in a reasonable time appeared unlikely. 2-D cross-section analysis, on the other hand, allowed a design refinement in just over an hour. The first filter constructed tuned to better than 20-dB return loss and 0.1-ns delay, uniformity.

Example 6—Coplanar Circuit Elements: In coplanar waveguide (CPW), ground equalization straps are often used for suppressing undesired modes. Fig. 20 shows a ground strap implemented in GMIC and drawn using Xgeom. The crossover used to join the ground surfaces introduces mismatch in the transmission line, which can be improved by narrowing the underpass at the crossover. This structure can be optimized for match by either deriving an equivalent circuit or optimizing automatically through the use of OSA's Empipe.

Fig. 21 shows an equivalent circuit of the crossover discontinuity derived from Sonnet generated S-parameter data at three frequencies and for three different widths of the underpass, 20, 40, and 60 μm. The solid line is a straight line fit passing through the origin and the data points represent values of the T-equivalent circuit derived from the S-parameters of the Sonnet simulations at three discrete frequency points. Clearly the discontinuity behaves like a lumped T-equivalent circuit with shunt capacitance and series inductances for all of the three widths. Since the structure is symmetric, the left and right reactances are equal in magnitude. The excess susceptance over that required for match is given by

$$B - \frac{2X}{1+X^2}.$$

This expression is plotted in Fig. 22 at 76.5 GHz as a function of the underpass width implying an optimum width of about 44 μm.

Optimization of the underpass width can also be achieved through Empipe. After the initial setup time in Empipe (of about 1–2 h), the automatic computer optimization of the underpass width occurs in about 35 min. Since the optimization stores all the simulations in a database, it is relatively easy to analyze the effect of process variations such as 20% variation in crossover height. Both the optimized underpass width and

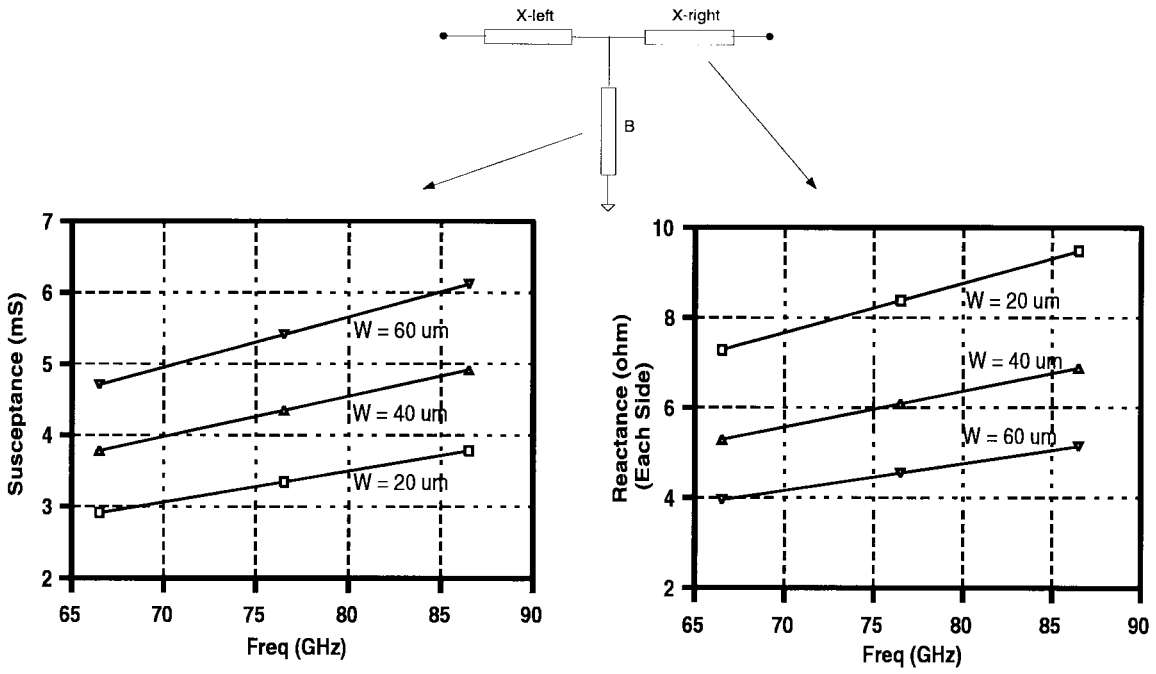


Fig. 21. Equivalent circuit of the ground equalization straps.

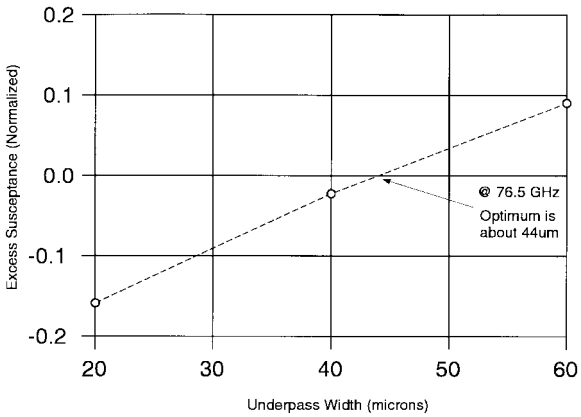


Fig. 22. Excess susceptance of grounding strap. Abscissa at zero crossing gives the optimum underpass width.

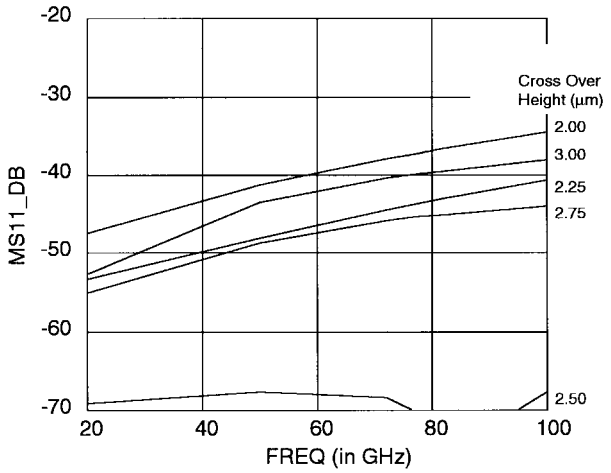


Fig. 23. Simulated return loss with Empipe optimized underpass width versus frequency. The crossover height is varied from 2.0–3.0 mm to study the effect of process variance.

the response with various crossover heights are very useful for circuit design centering. Fig. 23 shows return loss using the optimized value of the underpass (42.2 mm) using Empipe. Additionally, the crossover height was varied by ±20% as typically expected in a manufacturing process. Despite the process variation, the simulations show that the return loss remains acceptable.

The above example shows that in some situations derivation of an equivalent circuit may be sufficient for circuit optimization. Fig. 24 shows a CPW bandpass filter required to have a passband at 77 GHz and greater than 15-dB rejection below 20 GHz. Derivation of an equivalent circuit for this filter was likely to be time consuming and, therefore, automatic optimization directly in Sonnet using Empipe was preferred. Fig. 25 shows the optimized filter response along with the corresponding parameters.

Example 7—A 26-GHz 3-dB Backward Coupler: Use of a Lange coupler as a 3-dB backward coupler for high-frequency (HF) (greater than 25 GHz) applications in GMIC is deemed to be risky. This is because of parasitic crossover couplings and significant asymmetry in the crossover paths due to the short wavelength. Since a magnetic coupling coefficient of more than 0.7 with two coupled lines requires fine photolithography, implementation of a 3-dB backward coupler is difficult. This example provides a design of a 3-dB backward coupler at 26.5 GHz.

The maximum reasonable magnetic coupling attainable in glass using two coupled lines is about 0.65. To increase the effective magnetic coupling of two microstrip lines, capac-

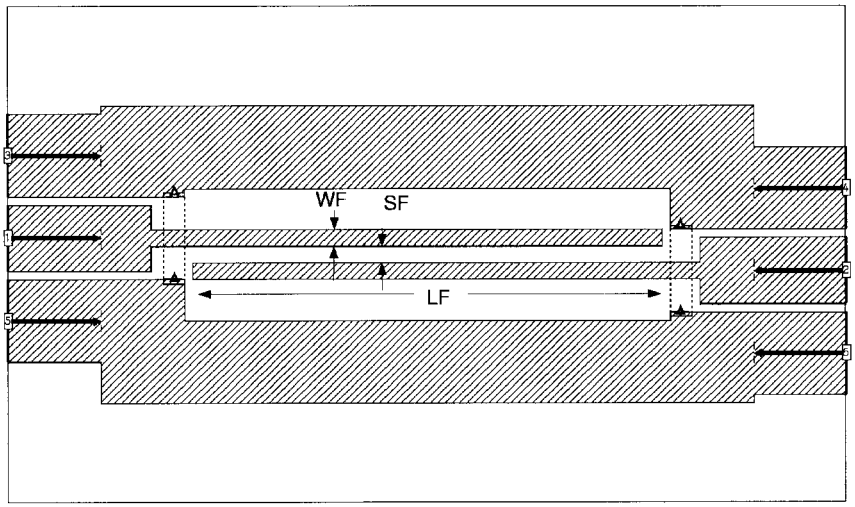


Fig. 24. Layout of a CPWG filter for 77-GHz applications.

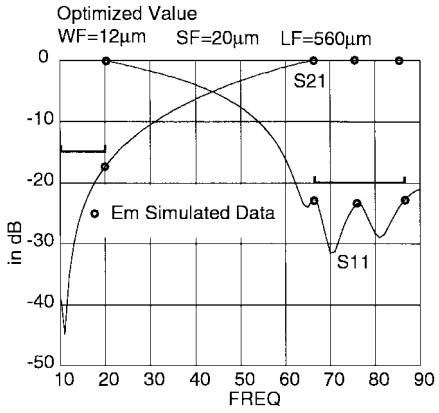


Fig. 25. Simulated performance of Sonnet/Empipe optimized filter shown in Fig. 24. The circles represent Sonnet data while the solid curves represent interpolated S-parameters.

itive coupling is introduced between isolated ports of the coupler. Fig. 26 shows this schematically together with the frequency response of the 3-dB backward coupler. This circuit is converted to the Xgeom layout shown in Fig. 27. The line widening at each port provides the extra shunt capacitance for the narrow coupled lines required for the maximum possible magnetic coupling for the allowable spacing. The crossover in the center switches the isolated port to the same side as the input port, allowing easy incorporation of the coupling capacitor to increase the effective magnetic coupling. Capacitive coupling between the lines is increased by a lumped MIM capacitance between the input and coupled ports. Because of the HF, parasitics in the circuit dominate and EM modeling is required.

The Xgeom layout shown in Fig. 27 was simulated and the S-parameters for five frequency points were used to extract the lumped equivalent circuit shown in Fig. 28; the extraction process of the equivalent circuit is explained in more detail in Appendix II. The fit was good as demonstrated by magnitudes of less than 0.02 in the vector difference between the S-parameters from the equivalent circuit and those from the Sonnet simulations. The analysis indicated the need to increase the capacitance to ground at the ports and, since the diagonal capacitive coupling was low, the gap length was increased by a meander. Finally, the length of the coupled section was made variable to tune the circuit to the specified frequency. This structure was set up for Empipe and run to optimize the dimensions shown in Fig. 29. Fig. 30 shows the final performance of the optimized coupler including losses. The optimized response shows wider bandwidth compared to the idealized response in Fig. 26 because the additional parasitics of the physical structure helped equalize the odd and even mode delays. The optimization time was about a week once the goals were properly defined—amply justified by the six-fold reduction in circuit area from the branchline configuration originally implemented.

IV. Creation of Library Elements

In many MW and MMW circuits, scalable models for individual circuit elements are required because at these frequencies parasitics are very important and the final adjustment of the circuit is invariably accomplished by a gradient optimization. As circuits continually push performance boundaries, each requires new libraries of unique elements as dictated by the specifications. Since such libraries are often circuit specific and the circuits have short turnaround time, model extraction from measurements on library wafer runs is usually impractical and expensive. In such situations, library models based on EM simulation may provide the only realistic solution. In this section, two examples of library element derivation and use are shown.

The first example in this section considers a matched SPDT switch with 10 W of power handling. The key goal here was to achieve reduction in circuit size without performance sacrifice. Since the turnaround time was short, a new scalable tapped inductor model was developed and successfully used in the

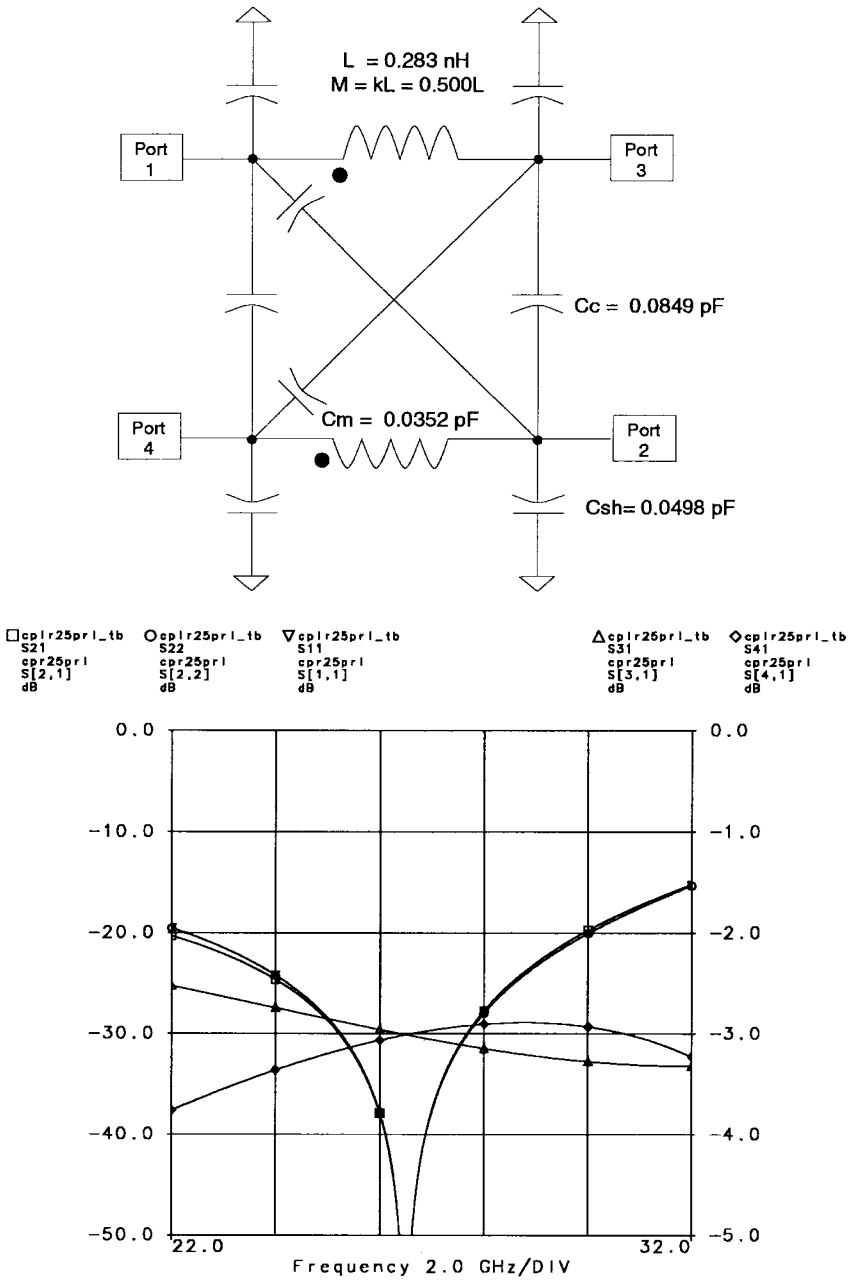


Fig. 26. Schematic of a simple circuit illustrating that the capacitive coupling between the noncoupled port and input port can increase the effective inductive coupling.

circuit. The second example considers a scalable composite shunt capacitor model.

Example 8—Tapped Inductors DC-18 GHz: A simple meander of a transmission line in an attempt to reduce the size of a circuit is not always successful. Adjacent sections of the transmission line give negative mutual coupling, reducing the overall effective self-inductance of the meandered line which in turn means longer and thinner total line length.

Fig. 31 illustrates a structure which accomplishes positive coupling between two adjacent line segments [17]. Given the approximate symmetry around port 1, this structure will be referred to as a (center-)tapped inductor. After an initial estimate of the line length using MDS's built-in models, it was decided to make a library element which had length dimension "len" varied between 46–76 mil with a third data point at 61 mil. The circuit element had 1110 subsections requiring 11 mbytes of RAM and took 37 min of CPU time per frequency point on an HP 735 workstation.

S-parameters generated by Sonnet's **em** were imported into MDS and all the post processing was carried out in that linear circuit simulator. The equivalent circuit for the tapped inductor is shown in Fig. 32. The lines are represented by two inductances capacitively loaded at the ends. To approximate distributed effects in the lumped element equivalent, inductors were incorporated in series with the shunt capacitors along with a negative capacitor in parallel with the line inductors.

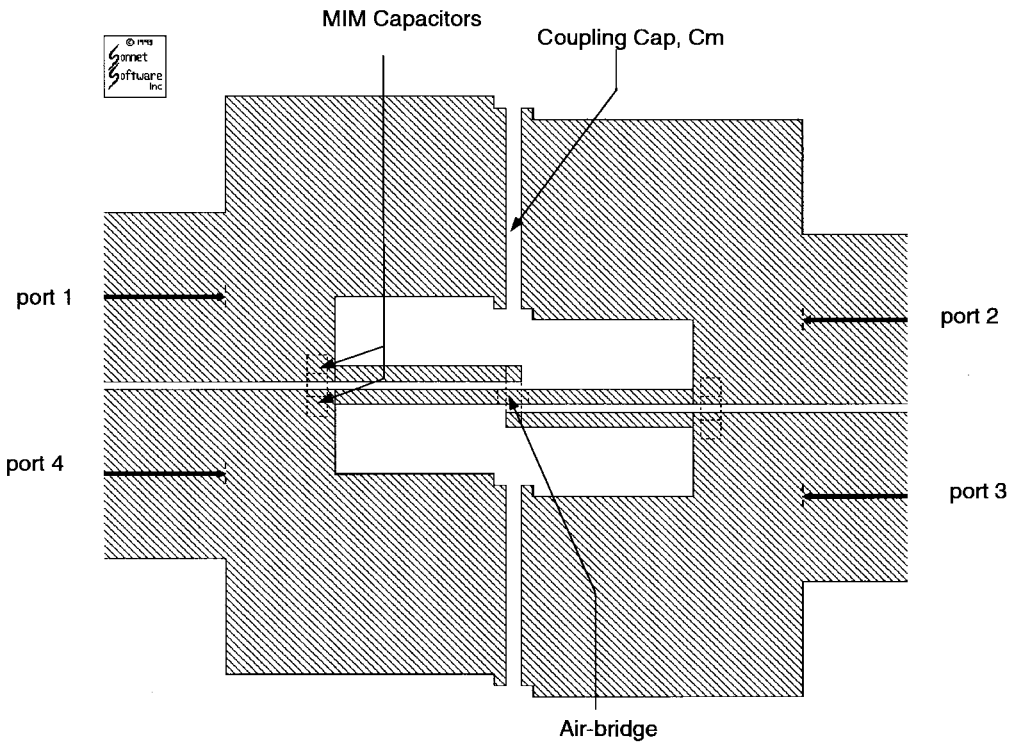


Fig. 27. Layout of 3-dB coupler at 27 GHz.

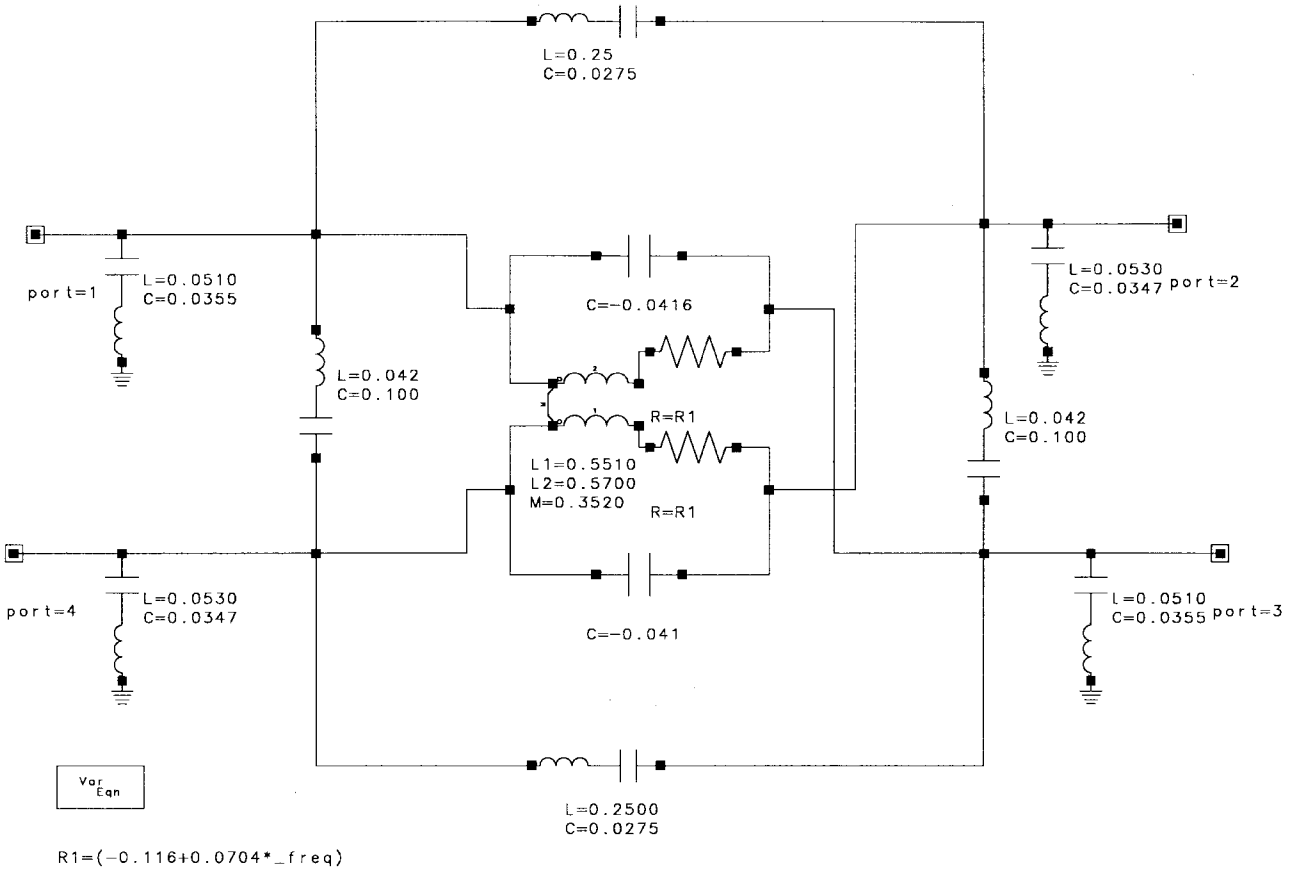


Fig. 28. Equivalent circuit derived from Sonnet simulation for the structure shown in Fig. 27.

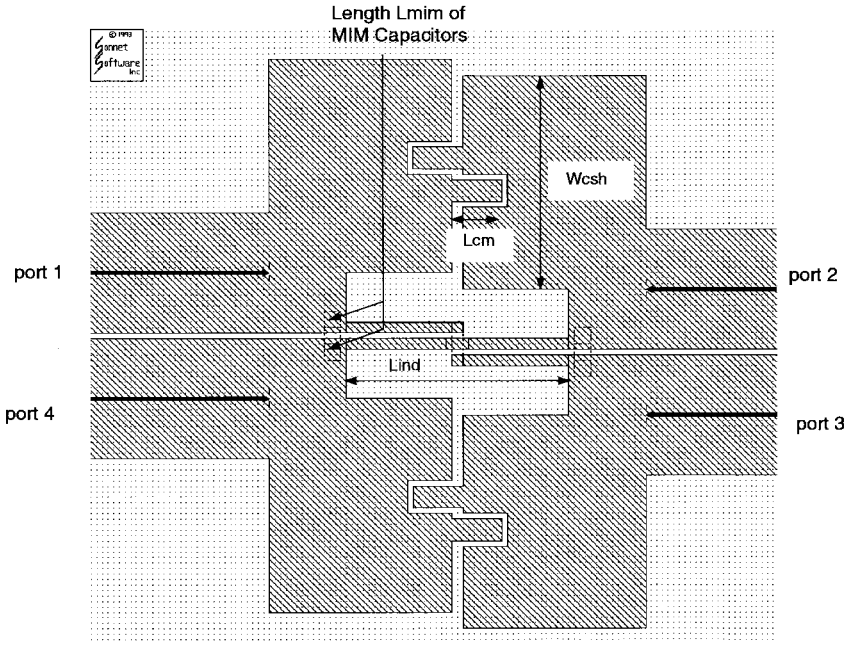


Fig. 29. Modified structure of the 3-dB backward coupler.

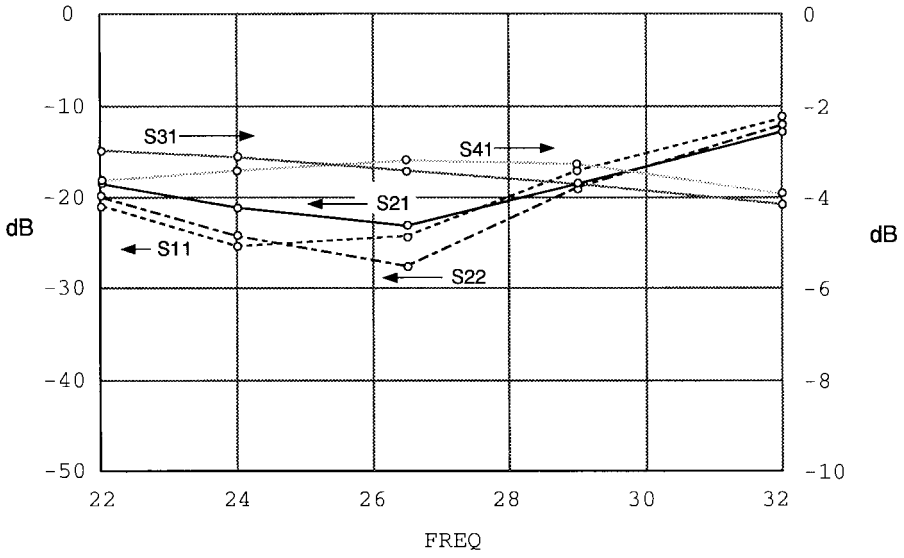


Fig. 30. Simulated optimized 3-dB coupler.

These nonphysical elements improve the fit of the model over a broad frequency range.

The S-parameters for symmetric excitation are obtained by joining ports 2 and 3 together and can be represented by the reduced equivalent circuit shown in Fig. 33. The S-parameters are transformed to Y-parameters and the three legs of the equivalent circuit are separated. Similarly, by using antisymmetric excitation, port 1 becomes a virtual ground and the S-parameters represent half of the circuit. Since the lines are only lightly coupled, the loss is well represented by a single resistance in series with the inductance.

Sonnet simulations were conducted from 1 to 21 GHz for the three sizes in steps of 2 GHz. The circuit elements are obtained by fitting the simulated equivalent circuit immittances to those extracted from the analysis of the Sonnet S-parameters. Since the equivalent circuit is representative of the physical effects underlying the structure, the interpolated data fits very well with the Sonnet simulations over the frequency of interest. Once the equivalent circuit elements for each length len were obtained, the values were fitted to a function of length by using the simple equations displayed in Fig. 32. Finally, Fig. 34 shows a close comparison between the MDS model simulated S-parameters and measured S-parameters between port 1 and 2 for len of 67 which represents an interpolated length.

The tapped-inductor model was utilized in the matched single pole double throw switch shown in Fig. 35. In the state

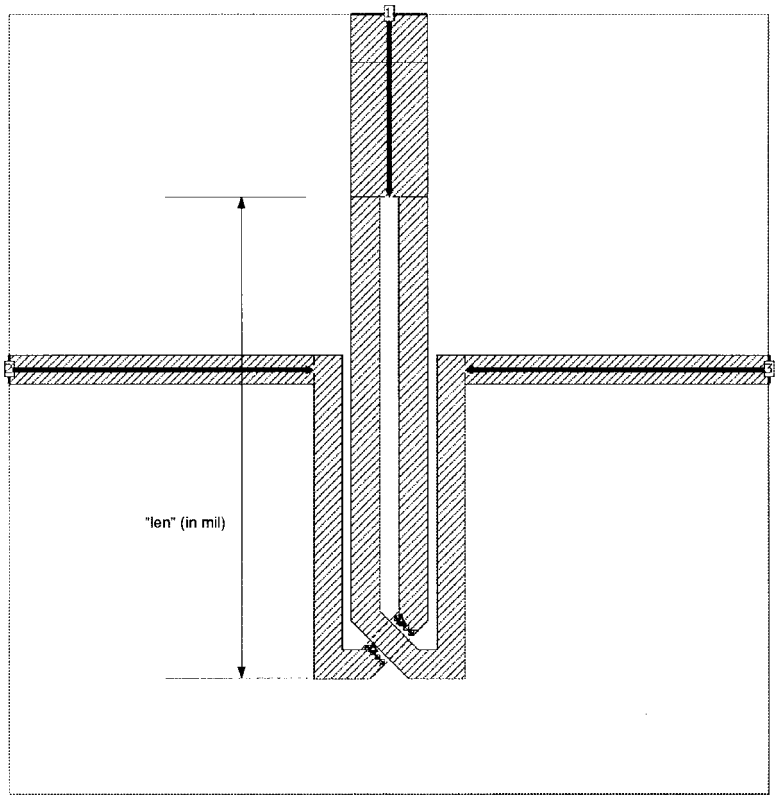


Fig. 31. Two adjacent lines configured to provide useful coupling. The structure is called the tapped inductor in this paper.

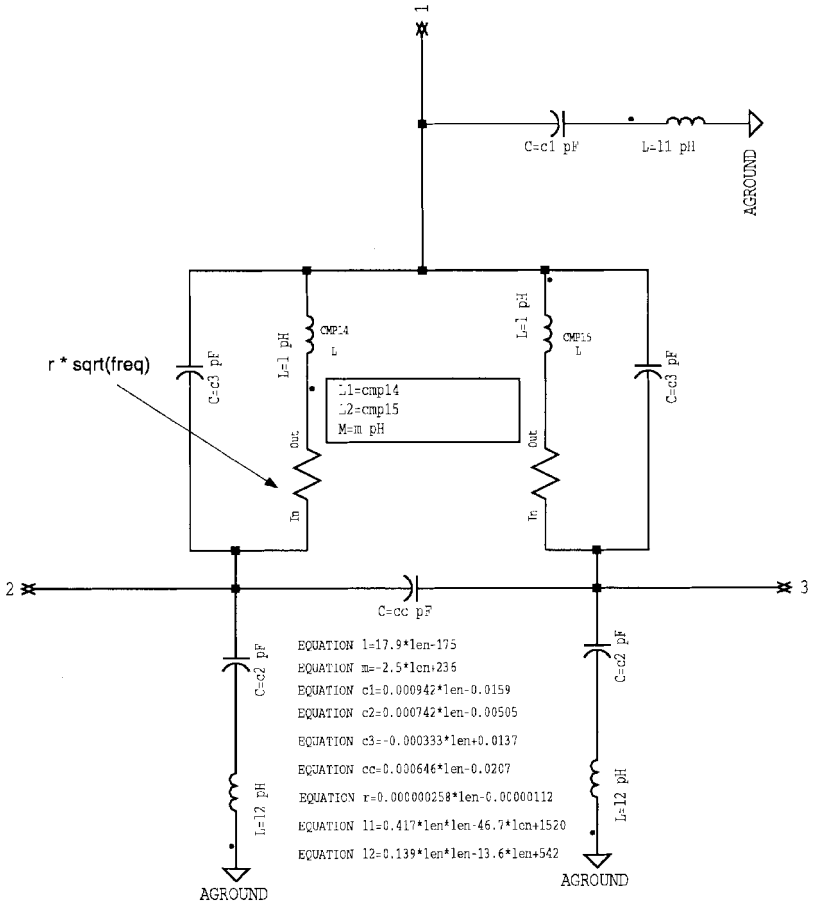


Fig. 32. Equivalent circuit for the tapped inductor. Note the various circuit elements are linearly scalable with len where $46 < \text{len} < 76$ mil.

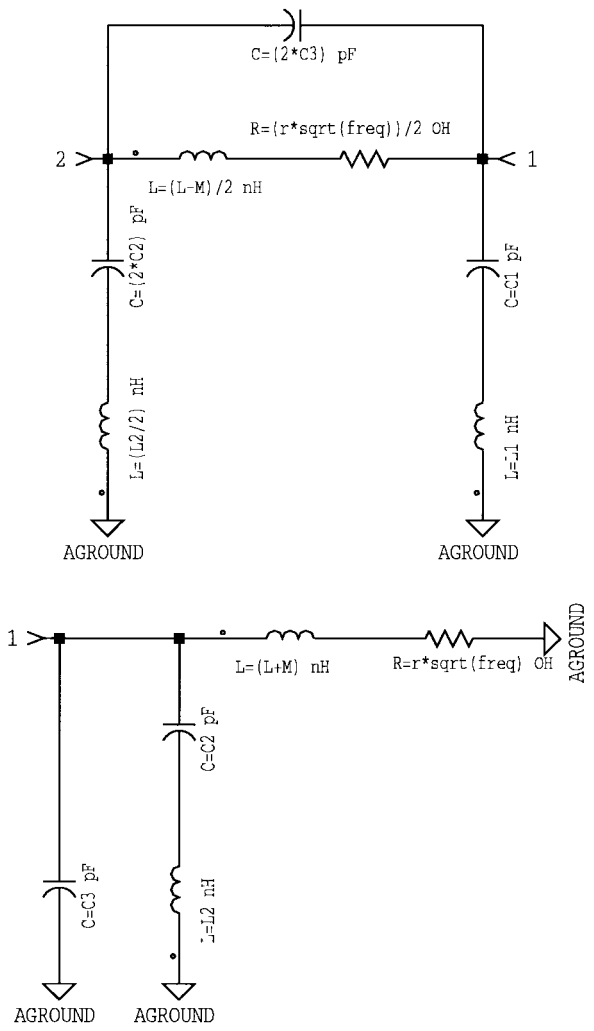


Fig. 33. Even- and odd-mode equivalent circuits for the tapped inductor. The even-mode equivalent circuit is obtained by combining ports 2 and 3, while the odd mode is obtained by exciting ports 2 and 3 out of phase and terminating port 1 in 50 Ω.

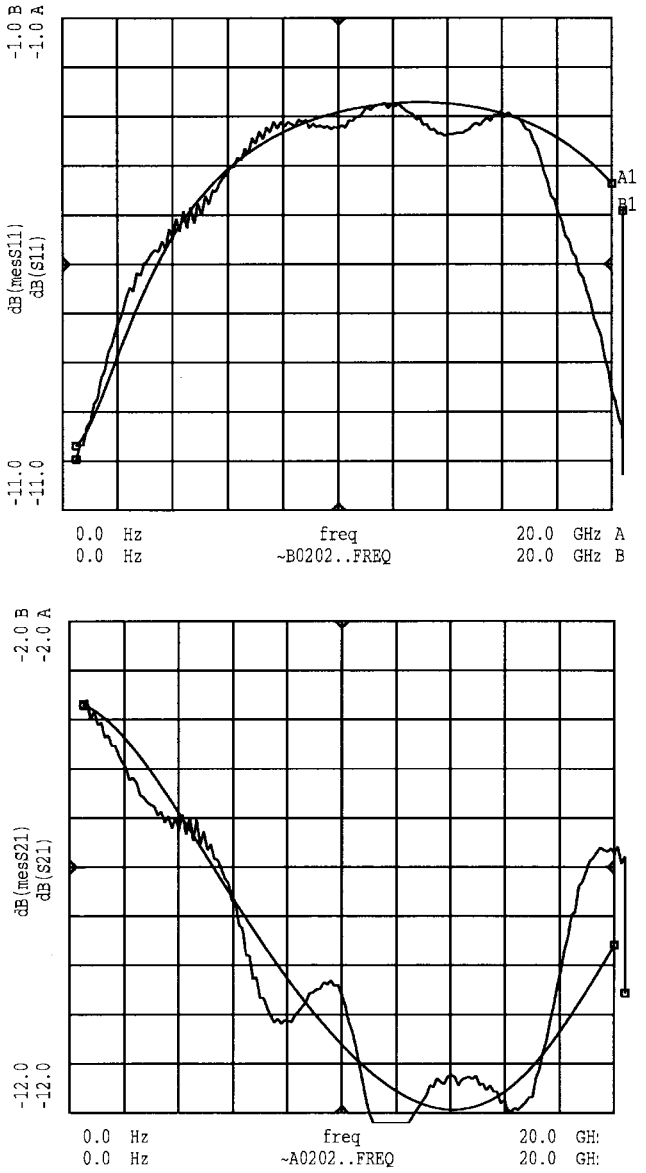


Fig. 34. Measured versus simulated magnitude of S_{11} and S_{12}. Phase for these parameters also showed very good agreement. Other S-parameters were similar with respect to the measurements.

shown in the figure, antenna A_1 is connected to the R_x port. The diode above A_1 is forward biased and transformed to an open circuit at the antenna A_1. Similarly, the diode below R_x is on and again transformed to an open circuit at the port R_x. By similar reasoning, antenna A_2 is connected to a 50-Ω load by the states of the diodes. Fig. 36 shows the measured and simulated response of the switch without any tuning.

Example 9—Composite Shunt Capacitor: The pedestals in the M/A-COM glass process are relatively big and provide low inductance to ground. The pedestals, however, also increase parasitic capacitances to ground. This final example shows how Sonnet's **em** can be used to model 3-D effects.

Microwave monolithic integrated circuit (MMIC) designs frequently use capacitance in the range of 0.2–0.5 pF. These capacitors are difficult for layout as they require huge interdigital capacitors or very small MIM's. Both of the approaches are difficult as they increase cost and reduce yields respectively. One well-known way to implement small capacitance is by putting two MIM capacitors in series. Fig. 37 shows such a structure. The two series capacitors are connected to a ground via to create a shunt capacitance that is in the of range 0.2–0.5 pF. The via, which is a conical structure, is implemented by two vertical vias of different area by splitting the substrate into two identical layers to represent the total substrate thickness. The validity of such approximations [12] has been previously demonstrated.

Again, to cover the range of required capacitance, EM simulations were conducted with X, the length of the second capacitor, having values of 12.5, 25, and 50 μm. The structure was de-embedded in Sonnet and the S-parameters for the three sizes were imported into MDS where they were transformed to Z-parameters. The equivalent circuit that was used to represent the MIM capacitors is shown in Fig. 38. The series inductances are negative because the de-embedding is carried out to the center of the structure as shown in Fig. 37. Since

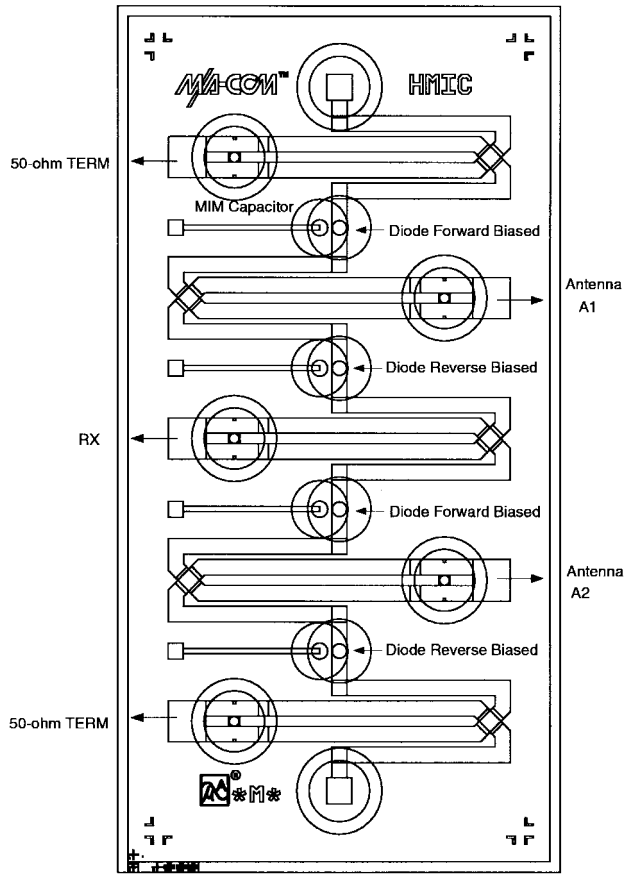


Fig. 35. The single pole two-throw switch utilizing tapped inductors.

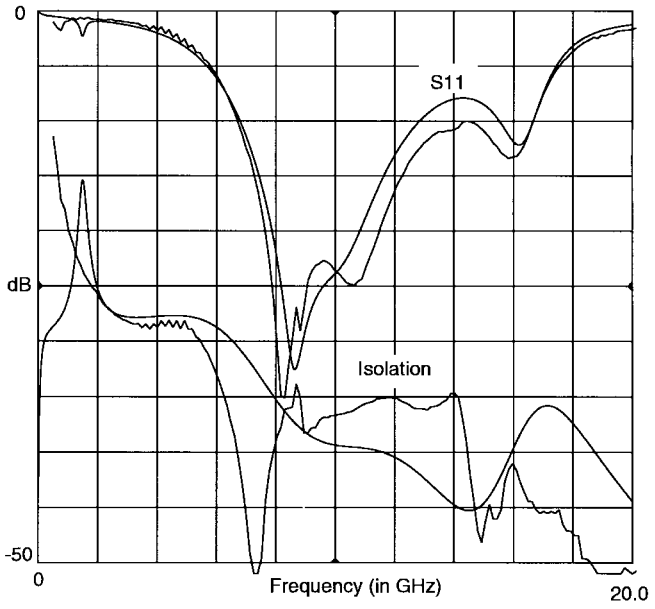


Fig. 36. Measured and simulated performance of the single-pole two-throw switch. Other samples showed similar agreement.

the X variations are only a slight perturbation in the overall structure, the shunt capacitance (which changes with X) is the only variable parameter as verified by the equivalent circuit extraction.

Fig. 39 compares the Sonnet simulated impedances of the T-equivalent circuit with those generated from the fitted equivalent circuit. The imaginary components match well while the real components show random deviations. This is also representative of other values of X.

Fig. 40 shows the variation of reciprocal capacitance versus the reciprocal length. This is the expected relation because the capacitors are in series and one of the capacitances varies proportionally to X. This library element has since been used very successfully in many circuits [16].

V. Conclusions

Contemporary MW and MMW circuits have benefited tremendously from EM simulations. However, with increased EM problem sizes, computer resources are becoming more stressed. By proper choice of the method for using EM simulators, considerable time and resources can be saved. The first choice of EM analysis should be a single-shot nonoptimizing analysis. This requires careful isolation of the unknown circuit element from the known circuit elements. When the performance of a circuit element is critical for the overall performance of the circuit, one has to resort to judicious circuit element optimization using either manual or automated methods depending on whether the problem requires structural or dimensional changes. It is important to realize that any optimization assumes the existence of a solution, which may not always be the case. Finally, when similar structures are being used in many different instances or circuits, (or being used as library circuit element), then deriving scalable models which have physical scaling rules have proved to be very useful. Optimization and extraction of scalable equivalent circuits have benefited from the equivalent circuit extraction technique outlined in Appendix II.

In all EM simulations, it is very important to reduce the simulation time required for any analysis. Besides the standard methods such as planes of symmetry, lossless metal, and larger subsections in unimportant regions, it has been found that removing sources of zeros and poles from a transfer function can tremendously speed up calculations as this lowers the number of frequency points required. In the example of the tapped inductor, the device was analyzed as a three-port element even though in the real application one of the ports is shorted to ground, introducing a pole in the transfer function. This technique can be exploited for filters with sharp responses where multiport analysis may be preferred (as this may remove the poles and zeros in the transfer function) instead of the actual two ports.

The success of EM simulations has encouraged individuals to attempt rather ambitious multilevel circuit designs. Representative structures that are currently being proposed for use with MW and MMW applications are illustrated in Fig. 41. The figure shows at least three steps of benzocyclobutene (BCB) over the present glass process and planar processing at all of these layers. Additionally, flip-chip technique is utilized to reduce parasitics and bonding problems. The EM

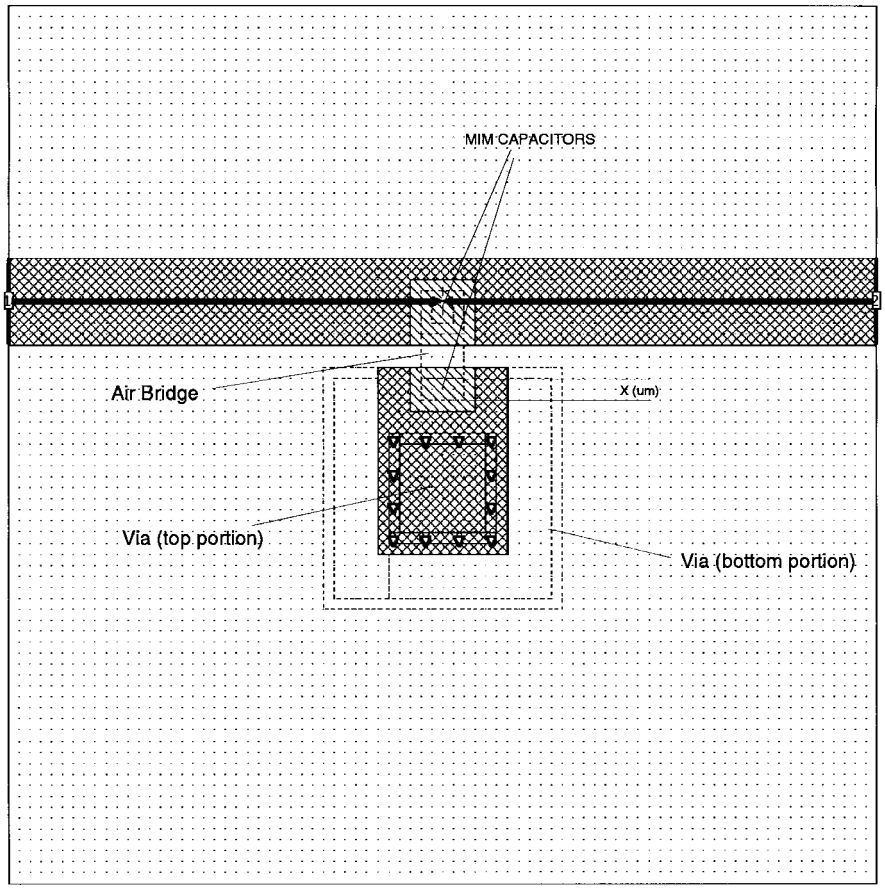


Fig. 37. Low-capacitance shunt capacitor implemented using two series MIM capacitors.

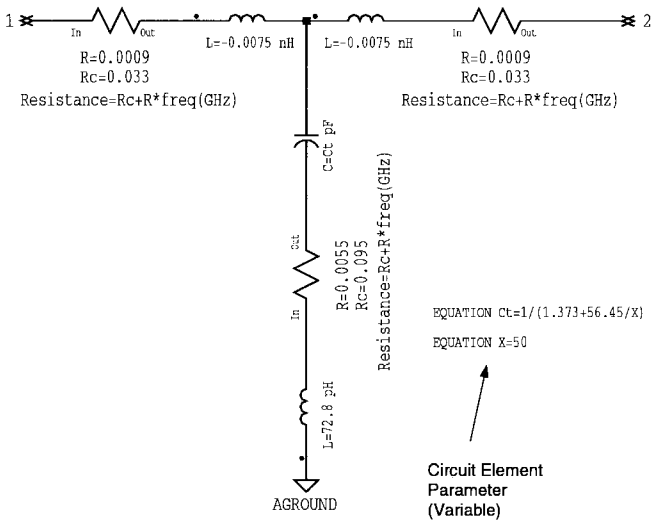


Fig. 38. Equivalent circuit for the shunt capacitor that is illustrated in Fig. 22.

problem size will grow tremendously as individuals continually push for more compact and multilevel circuits requiring new features in the EM simulators. These features should include better model extraction programs attached to the EM simulators, greater use of parallel computing to utilize many computers as typically available over intra-office networks, and direct links to circuit simulators. HP's HFSS does allow $[S]$ to $[Y]$, or $[Z]$ transformation but has no even- and odd-mode analysis or port re-configuration algorithms once the solutions are calculated. Recent advances in the FDTD method are very exciting and, with the advent of multiprocessor computers, the authors believe that EM simulations will become a matter of course for all commercially viable circuit designs and optimizations.

APPENDIX I
GMIC CROSS SECTION

Fig. 42 illustrates the GMIC cross sections [8], [9].

APPENDIX II
EQUIVALENT CIRCUIT EXTRACTION

The technique proposed here avoids most of the well-known shortcomings of optimizing techniques used for equivalent circuit extraction while providing the added benefit of not requiring *a priori* guesses about the variation of resistive losses with frequency. After an overview of the theoretical background of the admittance matrix for a floating inductor array, the technique is presented and applied to Sonnet simulated S-parameters for the 3-dB directional coupler example mentioned in Section III.

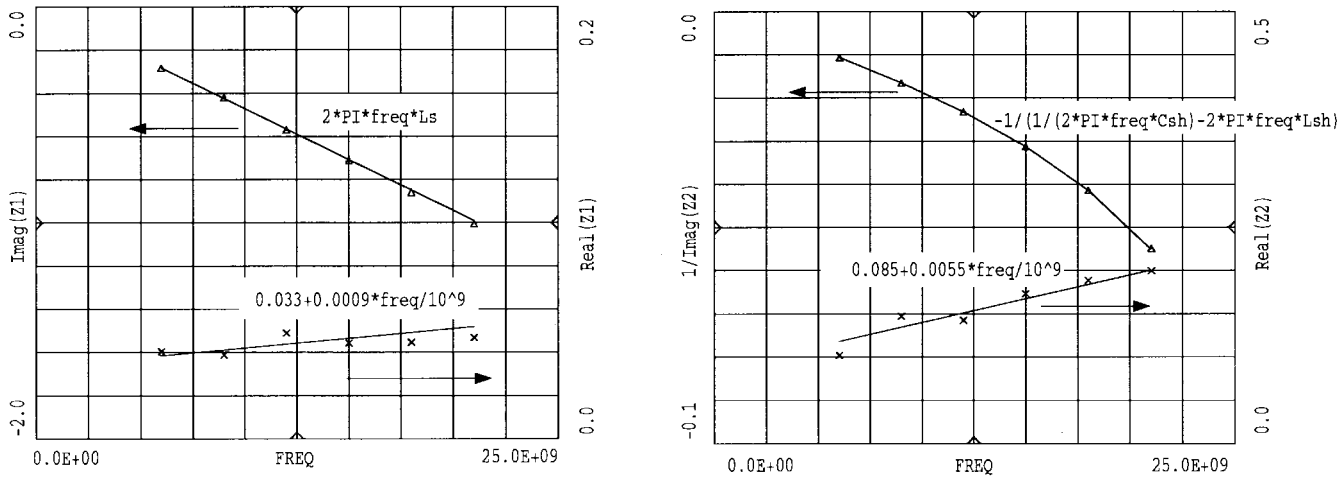


Fig. 39. Extracted impedances of the T-equivalent circuit from Sonnet's S-parameters are fitted over the frequency using the equivalent circuit in Fig. 37. The imaginary impedances from the equivalent circuit and Sonnet simulations are right on top of each other while the real impedance shows some difference.

A. Admittance Matrix for Floating Inductor Array

Begin with a simple array of N mutually coupled inductors arranged as shown in Fig. 43, with mutual inductances L_{ij} between L_i and L_j while L_{ii} is the self-inductance of L_i. If port i is now driven with voltage V_i while all other terminals are grounded, one has in terms of the port currents

$$V_i = s\sum_{j=1}^{N} L_{ij}I_j \qquad \text{for } 1 \le i \le N, \qquad s = j\omega$$

$$V_i = -s\sum_{j=1}^{N} L_{ij}I_{j+N} \qquad \text{top right corner}$$

$$V_{i+N} = -s\sum_{j=1}^{N} L_{ij}I_j \qquad \text{bottom left corner}$$

$$V_{i+N} = s\sum_{j=1}^{N} L_{ij}I_{j+N} \qquad \text{bottom right corner.}$$

It then follows from solving for the currents that if L is an order N square matrix with elements L_{ij}, the indefinite admittance matrix for the inductor array is given by an order $2N$ matrix

$$Y = \frac{1}{s}\begin{pmatrix} L^{-1} & -L^{-1} \\ -L^{-1} & L^{-1} \end{pmatrix}.$$

The analysis is essentially the same if a resistor is placed in series with the inductor. For any number of inductors greater than two, the resulting expressions can be quite complex. Fortunately, one does not really have to deal with them in this form; it is, however, useful to keep the format in mind since ultimately the target is to extract the inductance matrix in accessible form.

B. Equivalent Circuit Extraction

Using the above along with the properties of indefinite admittance matrices, an algorithm for working from the usual

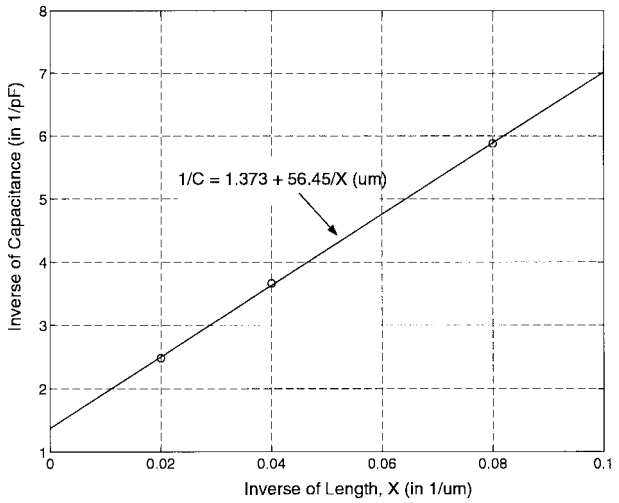


Fig. 40. The capacitance as function of the variable X. Circles are Sonnet extracted data while line is least square fit for the given function.

S-parameters to the details of an equivalent circuit can now be sketched out in the following steps.

Step 1, For each frequency, convert data from S-parameters to Y-parameters.

Step 2, Compute row sums and extract capacitances to ground. Subtract capacitive susceptance from diagonal elements. For inductors having overall conductor lengths which are significant fractions of a wavelength, accuracy is improved by using a series *LC* fit. If there is an actual inductance from a node to ground, remove just the capacitance by doing a parallel *LC* fit to the susceptance.

Step 3, Extract node-to-node capacitances by doing parallel *LC* fit to each off-diagonal susceptance. Add the capacitive susceptance to each term. Given no information to the contrary, the losses are left with the inductors; if there are real capacitors whose

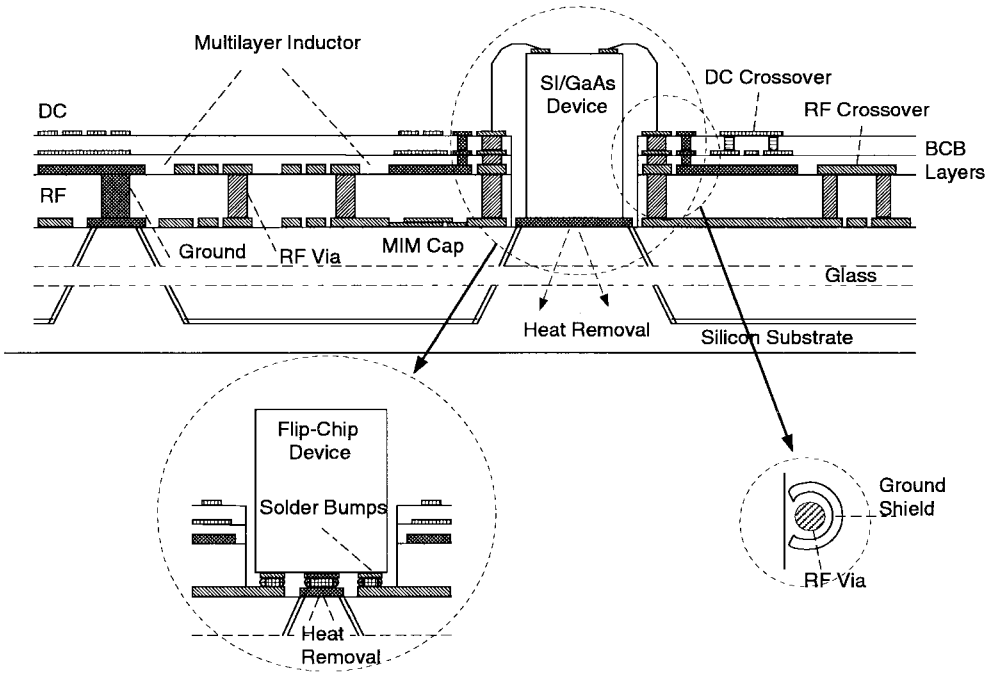


Fig. 41. Future process enhancements that will require full 3-D EM simulation. These are required from commercial considerations of cost reduction with performance enhancement.

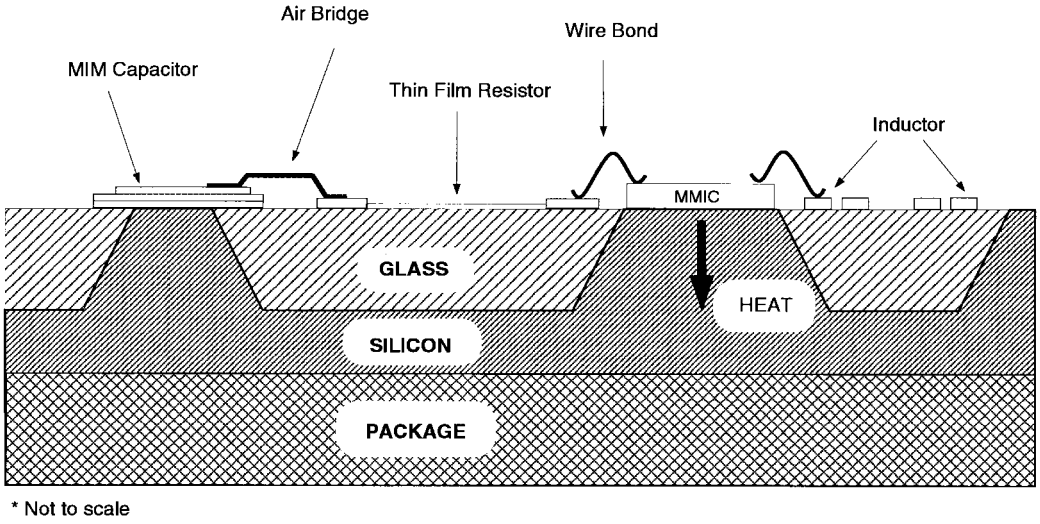


Fig. 42. GMIC cross section.

Q-factors are known, the corresponding parallel conductance can be accounted for as well.

Step 4, Isolate the proper submatrix and calculate its inverse. This yields an impedance matrix for the inductor array from which the resistance is obtained directly while the inductance is given by a fit over the desired frequency range to a straight line through the origin.

Step 4 may be clarified by recalling that the information is effectively replicated four times for the original array of inductors between pairs of ports. Connecting ports together or grounding them removes or combines some rows and columns while leaving undisturbed one of the original square

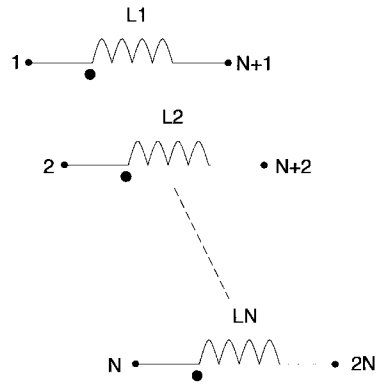


Fig. 43. N mutually couple inductors.

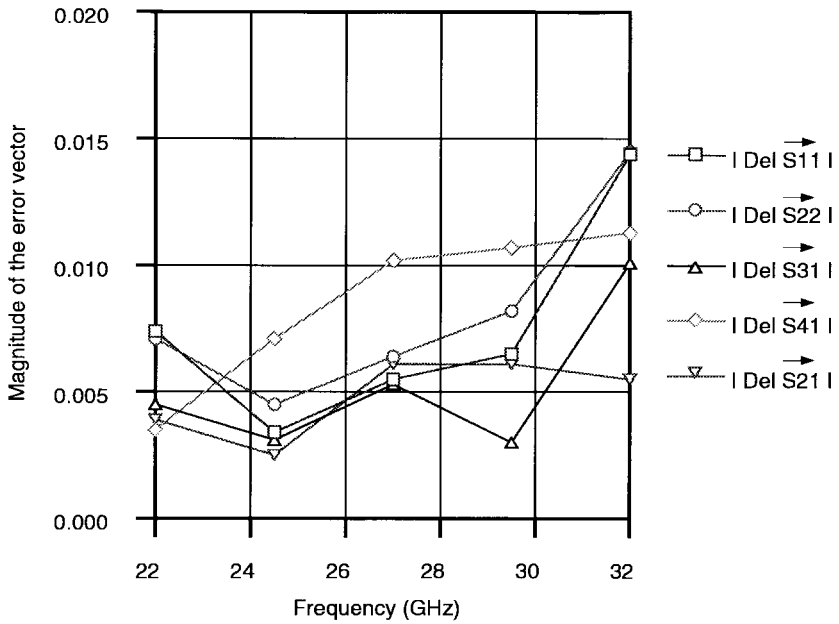


Fig. 44. Scattering parameter errors for coupler equivalent circuit.

submatrices which contains all the information remaining after the capacitances to ground are removed.

C. Application of the Technique to the 3-dB Backward Coupler

The circuit layout of the 3-dB backward coupler depicted in Fig. 27 was simulated in Sonnet. The S-parameters generated by Sonnet at 22, 24.5, 27, 29.5, and 32 GHz are first converted to Y-parameters.

On completion of Step 2 outlined above, a series combination of inductor and capacitor to ground is extracted at each port. The element values are forced to be symmetric by performing averaging to properly represent the electrical symmetry of the structure. Step 3 extracts the node-to-node capacitors, including series inductors where appropriate to better approximate distributed effects. These elements are also symmetrized as dictated by the circuit.

The remaining Y-matrix represents a coupled inductor pair. The impedance matrix is the matrix inversion of the proper isolated submatrix. The inductances are extracted by dividing the reactance by frequency, while losses are fitted to a linear function of frequency.

The extracted equivalent circuit is shown in Fig. 28. The calculated magnitude of the vector difference of the S-parameters generated by the equivalent circuit and that simulated by Sonnet for some of the pertinent S-parameters are shown in Fig. 44. The worst case error is less than 0.015 and the overall rms error is 0.008 supporting the accuracy of the extraction technique.

ACKNOWLEDGMENT

The coaxial surge protector example cited in this paper was analyzed by E. A. Soshea and his contributions are gratefully acknowledged by the authors. The authors additionally wish to thank Dr. P. W. Staecker, and G. C. DiPiazza who have greatly encouraged them during the course of this work.

REFERENCES

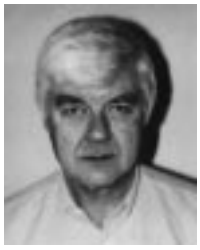
[1] R. Sorrentino "Modeling and design of millimeter passive circuits: From 2 to 3-D," in *24th European MW Conf. Proc.*, Cannes, France, Sept. 1994, vol. 1, pp. 48–61.
[2] XFDTD, Trademark of Remco Inc., State College, PA.
[3] Trademark of Sonnet Inc., Liverpool, NY.
[4] High Frequency Structure Simulator and Microwave Design System, Trademarks of Hewlett-Packard, Santa Rosa, CA.
[5] F. Alessandri, M. Mongiardo, and R. Sorrentino, "New efficient fullwave optimization of microwave circuits by the adjoint network method," *IEEE Microwave Guided Wave Lett.*, vol. 3, pp.414–416, Nov. 1993.
[6] F. Alessandri, M. Dionigi, R. Sorrentino, and M. Mongiardo, "A fullwave CAD tool of waveguide components using a high speed direct optimizer," in *1994 IEEE MTT-S Int. Symp. Dig.*, San Diego, CA, May 1994, pp. 1539–1542.
[7] Trademark of Optimization System Associates Inc., Dundas, Ont., Canada.
[8] P. Chinoy, N. Jain, P. Li, J. Goodrich, and C. Souchuns, "Manufacturing of low-loss microwave circuits using HMIC technology," in *1994 IEEE MTT-S Int. Symp. Dig.*, San Diego, CA, May 1994, pp. 1137–1140.
[9] R. J. Perko, R. J. Gibson, and C. Mattei, "MMIC versus hybrid: Glass microwave IC's and rewrite the rules," *Microwave J.*, no. 11, pp. 67–78, Nov. 1988.
[10] P. Onno, N. Jain, C. Souchuns, and J. Goodrich, "High power 6–18 GHz transfer switch using HMIC," in *1994 IEEE MTT-S Int. Symp. Dig.*, San Diego, CA, May 1994, pp. 79–82.
[11] J. White, *Microwave Semiconductor Engineering*. (Van Nostrand Reinhold Electrical/Computer Engineering Series), New York: Van Nostrand, 1982, pp. 315–387.
[12] N. Jain, "Engineering applications of electromagnetic field solvers," in *1994 IEEE MTT-S Int. Symp., Workshop Notes WMFA, Eng. Appl. Electromag. Field Solvers*, San Diego, CA, May 1994, pp. 61–77.
[13] J. W. Bandler, R. M. Biernacki, S. H. Chen, P. Grobelny, and R. H. Hemmers, "Space mapping technique for electromagnetic optimization," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 2536–2544, Dec. 1994.
[14] N. Jain and P. Onno, "High power 6-18 GHz switch designed in channelized wafer scale fabrication process," in *IEEE MTT-S Int. Symp. Dig.*, San Franciso, CA, June 1996, pp. 955–958.

[15] J. Goodrich and C. Souchuns, "HMIC—a fully capable silicon microwave integrated circuit process," in *Microwave USA Conf.*, Tokyo, Japan, Sept. 1993.
[16] C. Vatkanis, "First pass success in a complex X-band receiver optimizing intermodulation, noise, and power consumption by a combination of PHEMT and HBT technology," in *European Microwave Conf. Proc.*, Bologna, Italy, Sept. 1995, p. 658-662.
[17] M. E. Hines, private communication, Mar. 1988.
[18] W. J. Getsinger, "Coupled rectangular bars between parallel plates," *IRE Trans. Microwave Theory Tech.*, vol. MTT-10, pp. 65–72, Jan. 1962.
[19] J. H. Cloete, "Tables for nonminimum-phase even-degree low-pass prototype networks for the design of microwave linear-phase filters," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 123–128, Feb. 1979.
[20] Trademark of Ansoft Corporation, Pittsburgh, PA.
[21] N. Jain, "Automated circuit design using commercial EM simulators," in *1995 IEEE MTT-S Int. Symp., Workshop Notes WMFE, Automated Circuit Design Using Electromag. Simulators*, Orlando, FL, May 1995.

Nitin Jain (S'90–M'91) received the B.Tech degree in electrical engineering from Indian Institute of Technology, Madras, India, and M.S. and Ph.D. degrees in solid state electronics from the ECSE Department, Rensselaer Polytechnic Institute (RPI), Troy, NY, in 1986, 1989, and 1991, respectively.

Since 1991, he has been working at M/A-COM, Corporate R&D Center, Lowell, MA. He has authored 15 publications in international technical journals and holds one patent. His areas of interest include semiconductor device modeling, high-power switch design, passive circuit analysis, millimeter-wave circuit design, and EM modeling of passive circuits.

Dr. Jain was awarded the IEEE Student Fellowship from the MTT Society for his work on control MESFET's while he was a student at RPI.



Peter Onno (S'57–M'58) received the B.Eng. degree in engineering physics from McGill University, Montreal, Canada, in 1958. Following scholastic interruptions to work on airborne Doppler radar systems and navigation computers with Canadian Marconi Company, he received the M.Sc. and Ph.D. degrees in nuclear instrumentation from McGill University, in 1962 and 1965, respectively.

From 1964 to 1970, he worked at Bell Laboratories, on exploratory development for phased-array radars, planar circuit modeling, precision microwave filter design, and high-power phase shifters. Before joining M/A-COM, Corporate R&D Center, Lowell, MA, in 1983, he was involved in early cellular mobile telephone system development, ranging from instrumentation and programming for field studies through cell site diagnostics to cellular engineering software. More recently, he has worked on microprocessor controlled tunable filters, phase shifters and switches, microwave component models and libraries, and CAD tools. He has published seven papers and holds two patents.